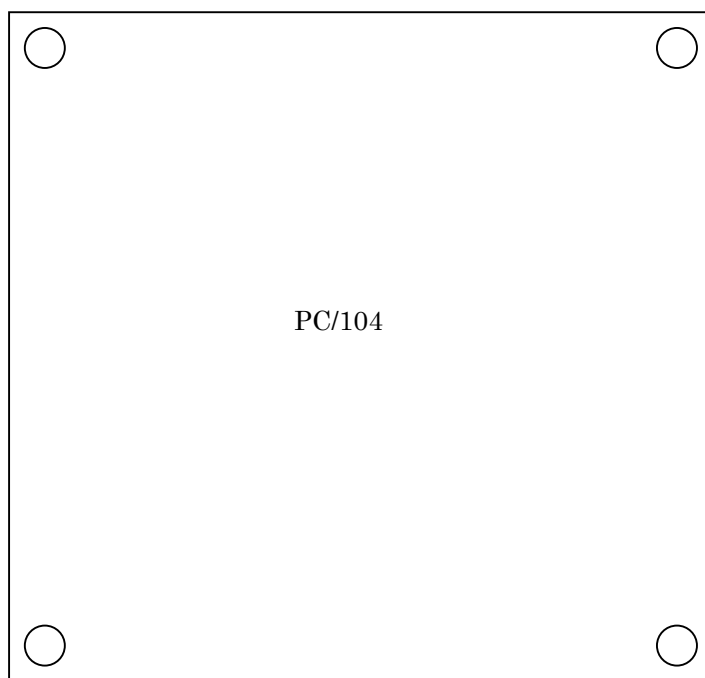


Real Solution for FA & LA



12bit 4ch Isolated Analog Output

QDA-724PC104

User's Manual

For MICRO SCIENCE

PC/104-BUS

DA-Board

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Mar 28, 2002

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Caution

Unpacking

This package contains a QDA-724PC104 board, and 4 pieces of 15mm stand-off. Upon receipt of the package, visually inspect the board for missing or damaged materials. This product was shipped in perfect condition as it was new. Examine the package for physical damage. In the event of damage, save all packing materials and notify your courier to validate shipping claims.

Anti-static discharge

The QDA-724PC104 contains components that are susceptible to static discharge, and should be handled with appropriate caution. The anti-static packing material protects components from being damaged by static discharge. Should the QDA-724PC104 board need to be returned for repair at a later date, it can be safely done by packing it in the original materials.

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A "PROGRAM" is a file or related group of files which may be loaded and processed on the user's computer or processing equipment to perform the functions.

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Customer Product Support Policy

MICRO SCIENCE will answer the written questions(including FAX,Email) in Japanese or English from the registered user about this product.

Send us the question form in this manual filled with the information.

We do not answer on phone with any language but Japanese.

Although MICRO SCIENCE may offer advice, we will not design the user's application.

Price List (# on Mar, 2002)

Items	Unit Price	Description
QDA-724PC104	\$ 430.00	12-bit / 4 out DA converter board for PC/104
User's Manual	\$10.00	Printed one. (PDF file is free for download from WEB)

The product consists of a QDA-724PC104 board and 4 pieces of standoff.

WEB : www.microscience.co.jp/eng/

Section 1. Introduction

1-1. Guide this Manual

This Manual contains a complete set of hardware and programming information for the QDA-724PC104 board, including configuration, installation, and I/O connection.

Section 1 contains the outline of functional descriptions, detail specifications, installation, and setup procedure for the board.

Section 2 contains the detail of analog output functions, and the digital data.

Section 3 contains the D to A update sequence.

Section 4 contains the calibration procedure, timing information for the external devices, trouble-shootings, and repair.

The last page is the request form for the Q and A.

1-2. Functional Specification

Analog Output	(typical unless otherwise noted and stated at 20 °C)
Number of channels	4 Outputs
Resolution / Code	12Bits (4096 counts) / Binary
Analog Output Range	$\pm 10\text{v}$ / 0 to +10v (software selectable)
Accuracy	$\pm 0.07\%$ FS
Non-Linearity	$\pm 0.004\%$ FS
Glitch	400 mv
Temperature Coefficient	$\pm 25\text{ppm}/^\circ\text{C}$
Settling time	16.5 micro-sec (10v swing to 0.1%FS on 100pF load)
Output Impedance	< 0.5 ohm
Driving Capability	5K ohm, 500pF
0v Output on Reset	Return to 0v on Reset Command or Power-on process.

Analog Output Mode (selectable with user program)

Asynchronous Update	Analog Outputs are updated independently by the software Command.
Synchronous Update	Analog Outputs are updated simultaneously by the software Command.

Control Elements for Synchronous Update with Multiple Boards.

Update Input	Analog outputs are updated synchronously by the specified edge of this input in the external synchronous mode. Also available for the general purpose interrupt input. (74HCT-type CMOS input with 10 K ohm pull-up.)
Update Output	Shot with the update timing in the synchronous mode. (74HCT-type CMOS output, 500ns width, negative polarity)

General Purpose Digital I/O

Input	2 bit (74HCT-type CMOS input with 10 K ohm pull-up.)
Output	1 bit (74HCT-type CMOS, latched output)

System Configuration

Bus Compatibility	PC/104 Bus All signals are driven or accepted with the C-MOS device. (74HCT type)
Board Address	Upper 12Bits: programmable by on-board switches. Lower 4Bits: on-board logic decoded for multiple I/O ports.
Interrupt	(selectable on-board switches if use)

I/O Connectors

Analog Output	16pin FRC type (2.54mm pitch)
Digital Input and Output	10pin FRC type (2.54mm pitch)

Physical, Environmental

Operating Temperature Range	0 to +55
Storage Temperature Range	-10 to +85
Relative Humidity	80% (Non-condensing)
Power Supply, Consumption	+5v 0.6 A

1-3. Functional Description

QDA-724PC104 is designed for multiple analog output channels, can not only update independently but also simultaneously analog output applications.

The board provides analog data up to 4 single-ended outputs.

The digital-to-analog converter has 12 bit resolution, and output range is software-selectable from 0 to +10v and -10 to +10v that specifies individually for each output.

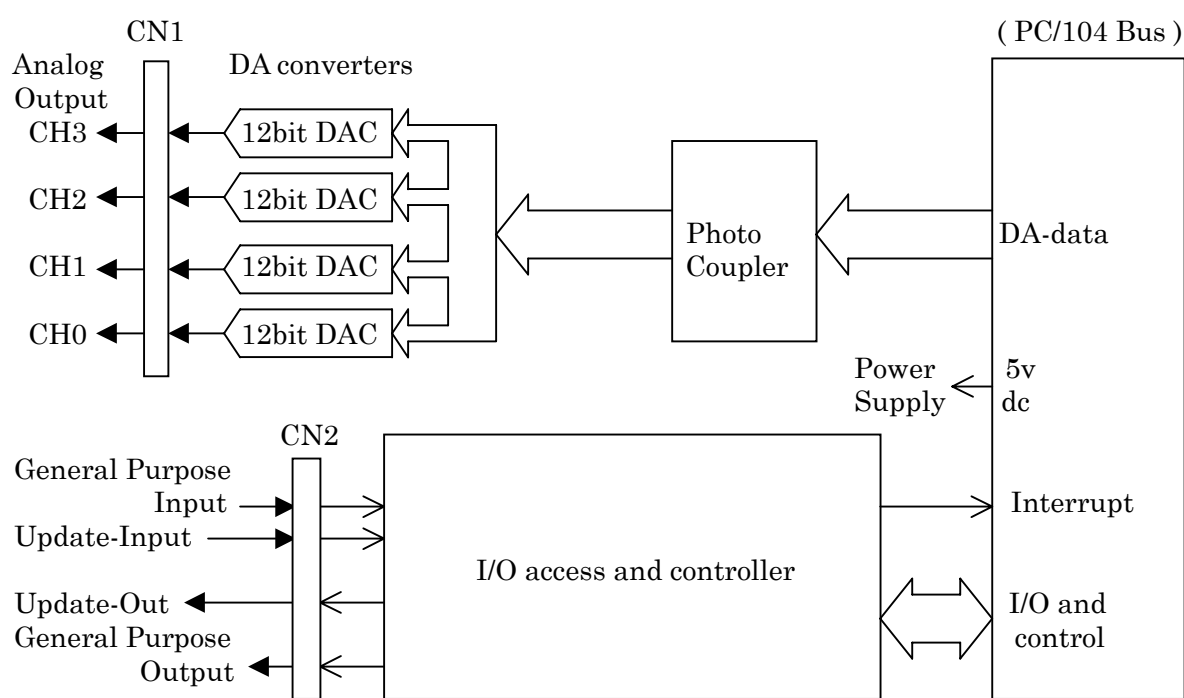
Analog outputs are commonly isolated by the photo-coupler against the PC/104 bus.

It is also available master-slave operation for multiple boards by the input and output of the timing. (Update input and output) The update input is also available for the general purpose interrupt with the software command.

Set the jumper-plug on the Interrupt level, if you use the function.

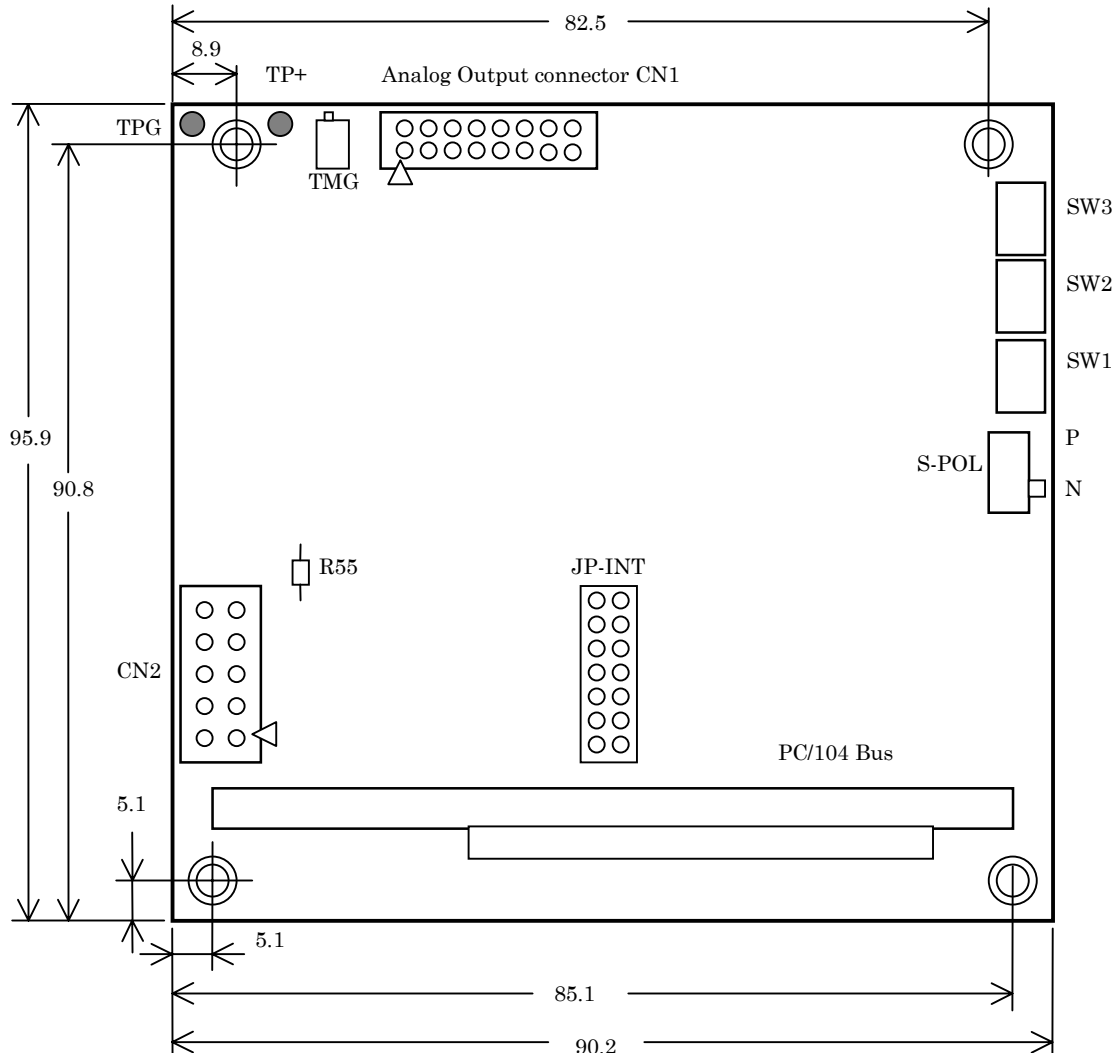
Because against the noise or cross-talk between Analog Output and Digital I/O, they are assigned for individual bracket. The base address of the board is programmable with the on-board switches.

Figure 1-3. Functional Block Diagram



1-4. Layout of the board

Figure 1-4.



Unit: mm

At shipping, on-board programmable elements are set to < > position.

SW1, SW2, SW3: Program switch for Base Address of the board. <0,1,E> / see 1-5-1./

JP-INT: Select jumper-switch for Interrupt Level. <NC> / see 1-5-2./

S-POL: Select switch for Polarity of General Purpose Output. <N> / see 1-5-3./

TP+: Test point for gain trimming, TPG: A-COM for test ground.

TMG: POT for gain trimming

R55: Pull up resistor for general purpose TTL digital output. (not assembled)

CN1: Connector for Analog Output (16pin, FRC) : shows the pin-1

CN2: Connector for Digital Input and output (10pin, FRC) : shows the pin-1



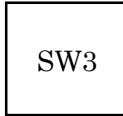
1-5. Settings on the board

1-5-1. BASE ADDRESS

QDA-724PC104 appears as a 16-byte block of registers within the host CPU's I/O address space. This address block must not conflict with other system I/O devices. You can program the on-board switches SW1, SW2, and SW3 as BASE ADDRESS of the board.

These hex-a-decimal defined switches are set to SW1=0, SW2=1, SW3=E at the factory of MICRO SCIENCE, that define the BASE ADDRESS to "01E0" hex. QDA-724PC104 occupies upper 16 byte address from the BASE. See section 3-3 for more information.

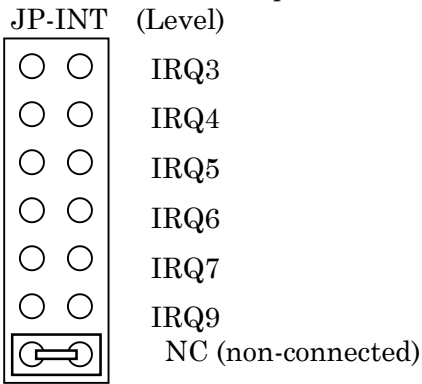
Figure 1-5A. Setting the BASE ADDRESS

Address Line →	AB15 to AB12	AB11 to AB08	AB07 to AB04	AB03 to AB00
On-board Hex-a-decimal → Switches				on-board logic decoded for multiple ports
Factory setting →	0	1	E	(F to 0)

1-5-2. Interrupt Level

Update input of QDA-724PC104 can cause an interrupt request to the CPU. Select the interrupt level by the jumper-switch "JP-INT", and program Write (BASE+2H) register to enable the input. See section 3-6 for the details.

Figure 1-5. select the Interrupt Level.



1-5-3. Polarity of Digital Output

QDA-724PC104 has 1 bit TTL level digital output for general purpose. Select the logical polarity of the output by the switch "S-POL".

This switch is set to "N" at the factory of MICRO SCIENCE that defines the logical polarity to "Negative". You can also switch to "P" for "Positive". See section 3-11 for the programming.

1-6. Analog Output Connector

Analog Outputs are available on a 16-pin FRC-type male connector CN1 on the board as illustrated in Figure 1-4.

The plug is also provided for general purpose, come with the board.

Figure 1-6. Analog Output Connector CN1 pin assignment

sign	/ Function /	pin assign		sign	/ Function /
CH0	Analog Output ch0	1	2	A-COM	/analog common/
CH1	Analog Output ch1	3	4	A-COM	/analog common/
CH2	Analog Output ch2	5	6	A-COM	/analog common/
CH3	Analog Output ch3	7	8	A-COM	/analog common/
		9	10		
		11	12		
		13	14		
		15	16		

<Note.1> A-COMs are Analog Common.

They are isolated against the digital ground “DG”.

<Note.2> On-board bracket : Model=HIF3FC-16PA-2.54DSA /made by HIROSE/
 Plug : Model=HIF3BA-16DA-2.54R(11) /made by HIROSE/

1-7. Digital Input and Output Connector

Digital Inputs and Outputs are available on a 10-pin FRC-type male connector CN2 on the board as illustrated in Figure 1-7. They are Update Input, Update Output, general purpose Input, and general purpose latched Output.

All Inputs are TTL current input level, and pulled-up with 10K ohm resistor.
All outputs are HCT-type CMOS level.

The plug is also provided for general purpose, come with the board.

Figure 1-7. Digital Input and Output Connector CN2 pin assignment

sign	/Function/	pin assign		sign /Function/
D0-IN	General Purpose Digital Input	1	○ ○	2 DG /Digital common/
D1-IN	General Purpose Digital Input	3	○ ○	4 DG /Digital common/
UPD-IN	External Update Input	5	○ ○	6 DG /Digital common/
UPD-OUT	External Update Output	7	○ ○	8 DG /Digital common/
Q0-OUT	General Purpose Digital Output	9	○ ○	10 DG /Digital common/

<Note.1> DGs are the Digital Common.

<Note.3> On-board bracket : Model= HIF3FC-10PA-2.54DSA / made by HIROSE /
Plug : Model= HIF3BA-10DA-2.54R(11) / made by HIROSE /

Section 2. Input and Output (details)

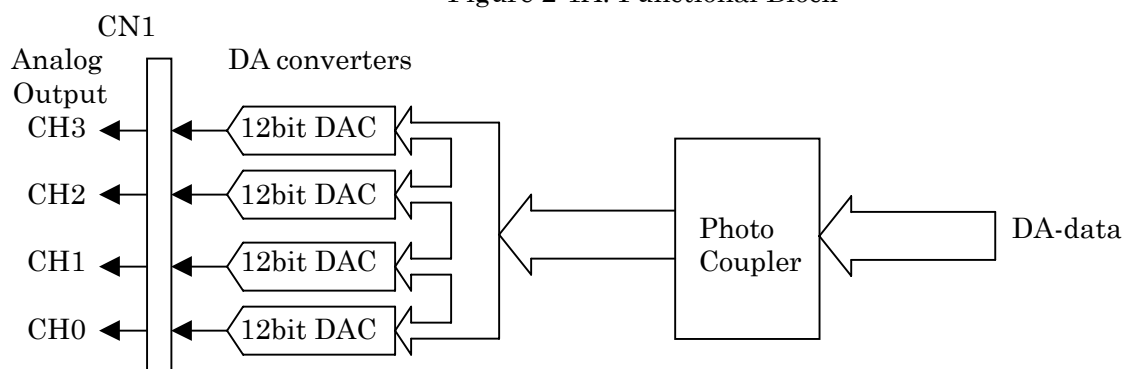
2-1. Analog Output configuration.

QDA-724PC104 has individual DA-converter and analog output circuit for each channel as illustrated in Figure 2-1A. On asynchronous output mode, each analog output are updated independently with the software command.

On synchronous update mode, all analog output are updated simultaneously with the software command.

All analog output are commonly isolated by the photo-coupler against the PC/104 bus.

Figure 2-1A. Functional Block

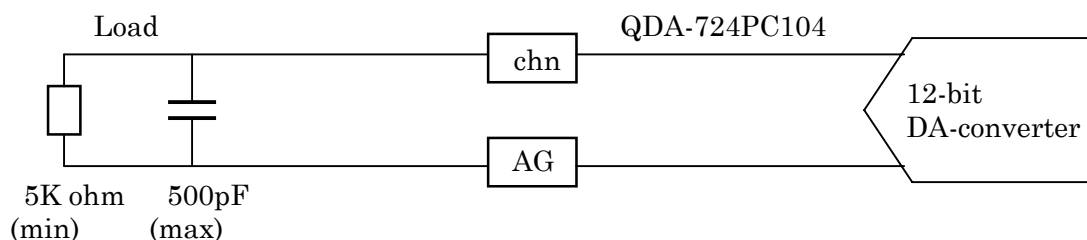


Drive-ability.

Each Analog Output can drive 5K ohm and 500pF load. Be careful for the capacity of the cable, load over 500pF cause trouble with un-stable output voltage.

Note, twisted-pair or sealed cable has 50-70pF for each meter.

Figure 2-1B.



2-2. Analog Output Range

Analog Output Range is selectable with the software command from 0 to +10v, and -10v to +10v.

The relation between DA-data and Analog Output voltage is follows.

Resolution.

$$\text{Res} = \text{Vspan} / 4096 \quad < \text{v/digit} >$$

Where Vspan is the width of the range.

For example, 20v for -10v to +10v range.

DA-data.

$$\text{Dda} = (\text{Vout} / \text{Res}) \quad \text{for Uni-polar Range.}$$

$$\text{Dda} = (\text{Vout} / \text{Res}) + 2048 \quad \text{for Bi-polar Range.}$$

Where Vout is the Analog Output Voltage.

Analog Output voltage.

$$\text{Vout} = (\text{Dda} \times \text{Res}) \quad \text{for Uni-polar Range.}$$

$$\text{Vout} = (\text{Dda} - 2048) \times \text{Res} \quad \text{for Bi-polar Range.}$$

Figure 2-2A. Uni-polar Output

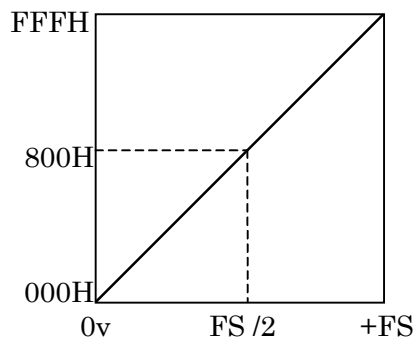


Figure 2-2B. Bi-polar Output

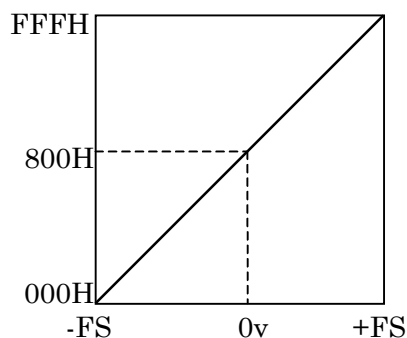
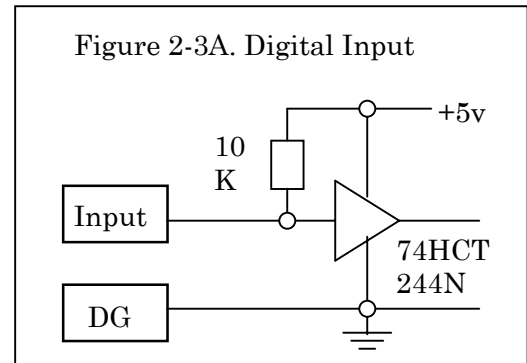


Table 2-2. DA-data vs Analog Output

DA-data	Analog Output <V>			
Hex (Decimal)	-10v to +10v	-5v to +5v	0 to +10v	0 to +5v
FFF (4095)	+9.99512	+4.99756	+9.99756	+4.99878
801 (2049)	+0.00488	+0.00244		
800 (2048)	0.00000	0.00000	+5.00000	+2.50000
7FF(2047)	-0.00488	-0.00244		
001 (0001)	-9.99512	-4.99756	+0.00244	+0.00122
000 (0000)	-10.00000	-5.00000	0.00000	0.00000

2-3. Digital Input and Output

All Digital Inputs are TTL level, and pulled-up to +5v with 10K ohm resistor.

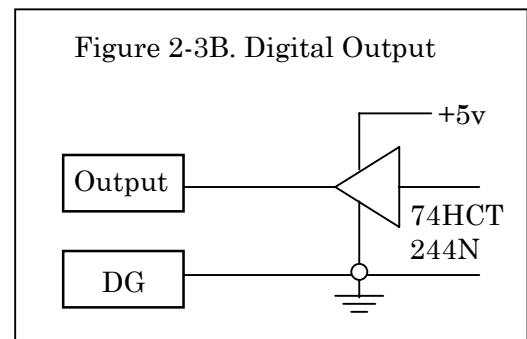


All Digital Outputs are HCT-type CMOS level.

General Purpose Output is latched output, and you can select the logical polarity by on-board switch S-POL.

MICRO SCIENCE set S-POL to “N” as Negative Logic, that cause the output to “TTL-High” level at power-on reset.

General Purpose Output does not clear by the software reset but clear by power-on hardware reset.



Section 3. General Programming

3-1. General Programming Information

Handling

QDA-724PC104 appears to the host PC/104 bus CPU as a block of contiguous 16 hardware registers mapped within the I/O address space.

These registers control the operation of QDA-724PC104 as long as they are accessed using 16bit I/O addressing with each 8bit data transfers.

These registers include Reset-board, Mode, Range, Interrupt, Status, DA-data, and General Purpose Digital I/O.

Operation

QDA-724PC104 does the updating analog outputs with the command.

These are explained in order as follows.

(section 3-2)

General updating sequences in Synchronous Mode and Asynchronous Mode.

(section 3-3 to 3-10)

The functions of each register. These are the elements for programming.

3-2. General Updating Sequence

QDA-724PC104 has two kind of operation Mode.
They are Synchronous Update Mode,
and Asynchronous Update Mode.
See follows for detail.

3-2-1. Analog Output Process

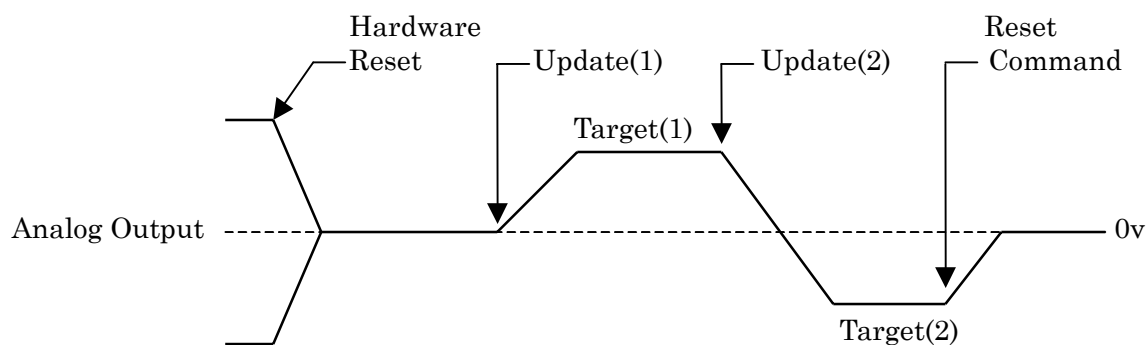
Reset Operation.

All Analog Outputs shall return to 0v on
Reset Command or Hardware Reset
process.

Update Process

On update operation, Analog Output shall
change to the new target value(=voltage) at
a speed of 4 volt/micro-second, then be in
stable 0.1% of Full-Scale within 16.5 micro-
second on 100pF load for 10v swing.
This is the **Settling Time**.

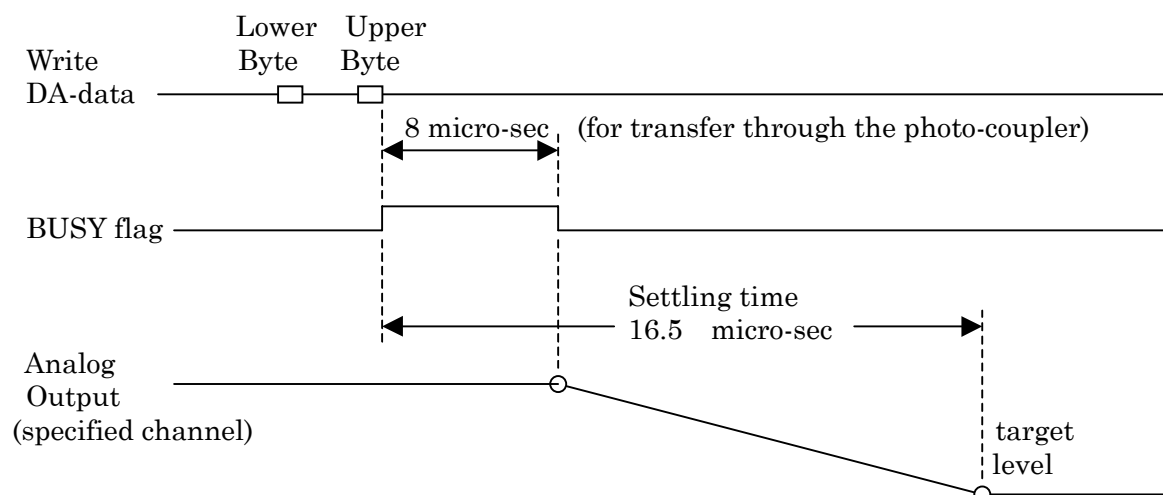
Figure 3-1A. Reset and Update process.



3-2-2. Individual Asynchronous Update operation.

In this mode, each Analog Output shall be updated Individually and immediately with the software command. See section 3-5 and 3-9 for programming.

Figure 3-2-2. Update a Channel.



Procedure.

```
Rst = inp (BASE+0x7) ; /* Reset the Board, "Rst" is ID of the board */
Outp (BASE+0x2, 0x0) ; /* set external control, see section 3-6. */
Outp (BASE+0x4, 0x0) ; /* set Asynchronous mode, see section 3-5. */
Outp (BASE+0x5, rng) ; /* set output range, see section 3-7. */
```

Then,

```
Outp (BASE+0x8, ch0-L) ; /* Lower byte data for Channel-0 */
Outp (BASE+0x9, ch0-U) ; /* Upper byte data for Channel-0 */
```

Or,

```
Outp (BASE+0xA, ch1-L) ; /* Lower byte data for Channel-1 */
Outp (BASE+0xB, ch1-U) ; /* Upper byte data for Channel-1 */
```

Or,

```
Outp (BASE+0xC, ch2-L) ; /* Lower byte data for Channel-2 */
Outp (BASE+0xD, ch2-U) ; /* Upper byte data for Channel-2 */
```

Or,

```
Outp (BASE+0xE, ch3-L) ; /* Lower byte data for Channel-3 */
Outp (BASE+0xF, ch3-U) ; /* Upper byte data for Channel-3 */
```

<Note-1> Write lower byte first then upper byte sequentially, and Analog Output word data on DA-converter shall be updated at the written timing of upper byte.

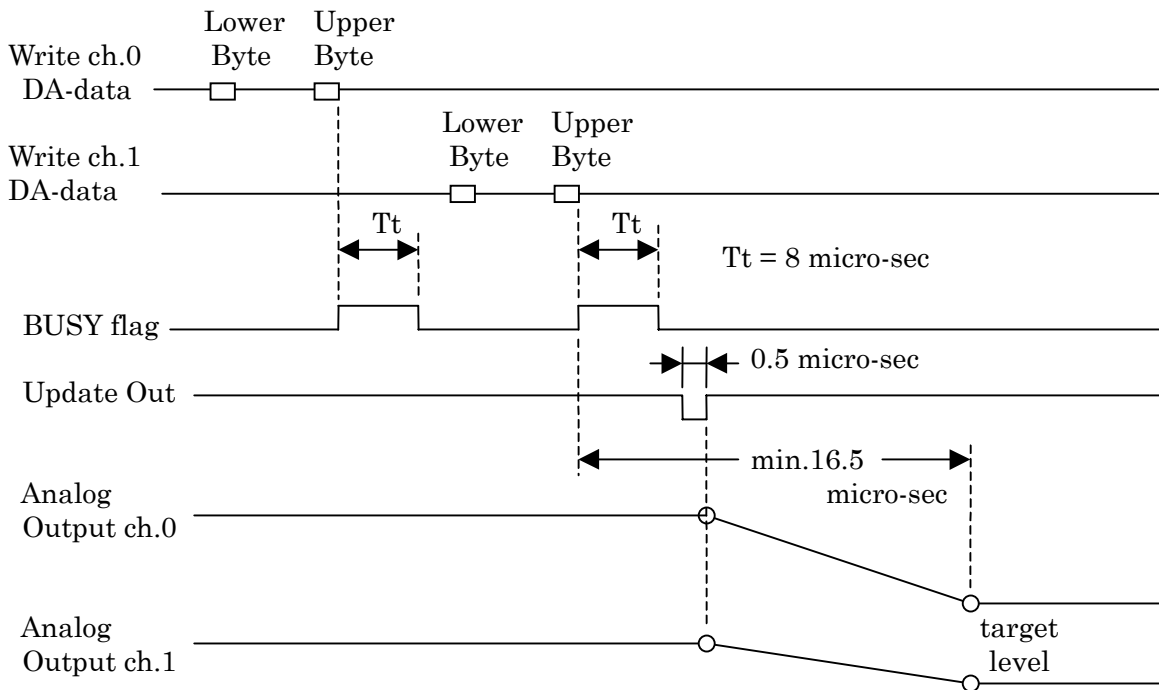
<Note-2> Write update data when the "BUSY" flag state is "Low". "BUSY" flag shall be set while the previous data is transferring through the photo-coupler.

3-2-3. Simultaneous Synchronous Update operation.

In this mode, all Analog Output shall be updated simultaneously with the software command.

See section 3-5 and 3-9 for programming.

Figure 3-2-3. Simultaneous Update all Channels.



Procedure.

```
Rst = inp (BASE+0x7) ; /* Reset the Board, "Rst" is ID of the board */
Outp (BASE+0x2, 0x0) ; /* set external control, see section 3-6. */
Outp (BASE+0x4, 0x80) ; /* set Synchronous mode, see section 3-5. */
Outp (BASE+0x5, rng) ; /* set output range, see section 3-7. */
```

Then,

```
Outp (BASE+0x8, ch0-L) ; /* Lower byte data for Channel-0 */
Outp (BASE+0x9, ch0-U) ; /* Upper byte data for Channel-0 */
Outp (BASE+0xA, ch1-L) ; /* Lower byte data for Channel-1 */
Outp (BASE+0xB, ch1-U) ; /* Upper byte data for Channel-1 */
Outp (BASE+0xC, ch2-L) ; /* Lower byte data for Channel-2 */
Outp (BASE+0xD, ch2-U) ; /* Upper byte data for Channel-2 */
Outp (BASE+0xE, ch3-L) ; /* Lower byte data for Channel-3 */
Outp (BASE+0xF, ch3-U) ; /* Upper byte data for Channel-3 */
```

Finally,

```
outp (BASE+0x7, upd) ; /* Simultaneous Update, "upd" is a dummy */
```

<Note-3> Write lower byte first then upper byte sequentially for all Channels, and all Analog Output word data on each DA-converter shall be updated simultaneously at the written timing of update command.

<Note-4> As same as Note-2 of previous page.

3-3. I/O Register Memory Map

QDA-724PC104 appears as a 16-byte block of registers within the host CPU's I/O address space. This address block must not conflict with other system I/O devices.

You can program the on-board switches SW1, SW2, and SW3 as BASE ADDRESS of the board.

These hex-a-decimal defined switches are set to SW1=0, SW2=1, SW3=E at the factory of MICRO SCIENCE, that specify the BASE ADDRESS to "01E0" hex.

QDA-724PC104 occupies upper 16 byte address from the BASE.

See figure 1-4 for the location of the board.

Figure 1-5A. Setting the BASE ADDRESS

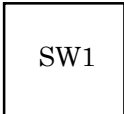

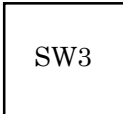
Address Line →	AB15 to AB12	AB11 to AB08	AB07 to AB04	AB03 to AB00
On-board Hex-a-decimal → Switches				on-board logic decoded for multiple ports
Factory setting →	0	1	E	(F to 0)

Table 3-3. QDA-724PC104 Register Assignment. (All the port consist of 8bit.)

I/O Address	Direction	Description	Refer to
BASE +FH	Read		
	Write	Upper Byte of Analog Output CH.3 (DA) Data	Section 3-9
BASE +EH	Read		
	Write	Lower Byte of Analog Output CH.3 (DA) Data	Section 3-9
BASE +DH	Read		
	Write	Upper Byte of Analog Output CH.2 (DA) Data	Section 3-9
BASE +CH	Read		
	Write	Lower Byte of Analog Output CH.2 (DA) Data	Section 3-9
BASE +BH	Read		
	Write	Upper Byte of Analog Output CH.1 (DA) Data	Section 3-9
BASE +AH	Read		
	Write	Lower Byte of Analog Output CH.1 (DA) Data	Section 3-9
BASE +9H	Read		
	Write	Upper Byte of Analog Output CH.0 (DA) Data	Section 3-9
BASE +8H	Read		
	Write	Lower Byte of Analog Output CH.0 (DA) Data	Section 3-9
BASE +7H	Read	Reset Board, and get ID.	Section 3-4
	Write	Analog Output Simultaneous Update control.	Section 3-9
BASE +6H	Read		
	Write		
BASE +5H	Read		
	Write	Analog Output Range	Section 3-7
BASE +4H	Read		
	Write	Analog Output Update Mode	Section 3-5
BASE +3H	Read	General Purpose Digital Input.	Section 3-11
	Write	General Purpose Digital Output. (latched)	Section 3-11
BASE +2H	Read	Status	Section 3-8
	Write	External update and/or interrupt input control	Section 3-6
BASE +1H	Read		
	Write		
BASE +0H	Read		
	Write		

3-4. Reset the Board, and get ID

```
rst = inp (BASE+0x7) ; /* Reset the Board */
```

Read (BASE+7H) Register cause the board reset.

All registers of the board must be initialized except for the last values of General Purpose Digital Output described in section 3-10.

The Update process shall be broken, and all analog output force to “0 volt”.

Where “rst” is the ID that depend on the board, “21H” for QDA-724PC104.

Table 3-4. Read (BASE+7H) Register Bit Field.

Bit	Description
B7	21H is the ID for QDA-724PC104.
B6	
B5	
B4	
B3	
B2	
B1	
B0	

3-5. Analog Output Mode

```
outp (BASE+0x4, mc) ; /* Analog Output Mode */
```

Write (BASE+4H) Register specifies the Mode for Analog Outputs.

Table 3-5. Write (BASE+4H) Register Bit Field.

Bit	Term	"=1" specifies	"=0" specifies	Reset
B7	Update mode	Simultaneous(Synchronous)	Individual(Asynchronous)	0
B6	Update timing	External "UPD-IN" Input	Software Command	0
B5	Not-Used.	Stay "0" in any mode.		0
B4				0
B3				0
B2				0
B1				0
B0				0

Bit <**B7**>:

See section 3-2 for the sequence of the operation.

Bit <**B6**>:

Where B6=0, execute timing of write (BASE+7H) register is the update timing. See section 3-9 for the sequence.
Where B6=1, write (BASE+2H) register specify the valid edge. See next section 3-5.

3-6. Update and/or Interrupt Input control

out (BASE+0x2, cnt) ; /* Control the input “UPD-IN” */

Write (BASE+2H) Register specifies the external input “UPD-IN” as an interrupt, valid polarity in Synchronous Update mode, and clear interrupt request flag.

See section 1-5 for interrupt level selection.

Table 3-6. Write (BASE+2H) Register Bit Field.

Bit	Term	“=1” specifies	“=0” specifies	Reset
B7	Control the input “UPD-IN” as an interrupt	Enable	Disable	0
B6	Valid edge of the external input “UPD-IN”	Rising	Falling	0
B5	Not-Used			0
B4				0
B3	Control the Interrupt request flag	Clear	Non-effect	0
B2	Not-Used			0
B1				0
B0				0

<Note>

Interrupt output to PC/104 bus is open collector with 1 K ohm pull-up, and 500 ns pulse width.

3-7. Analog Output Range

```
outp (BASE+0x2, rng) ; /* Analog Output Range */
```

Write (BASE+2H) Register specifies the analog output range for each channel individually.

Table 3-7. Write (BASE+5H) Register Bit Field.

Bit	Term	"=1" specifies	"=0" specifies	Reset
B7	Not-Used.			0
B6				0
B5				0
B4				0
B3	Analog Output Range for Channel-3	-10v to +10v	0 to +10v	0
B2	Analog Output Range for Channel-2			0
B1	Analog Output Range for Channel-1			0
B0	Analog Output Range for Channel-0			0

<Note>

Analog Output Range shall be updated when DA-data updated simultaneously.

3-8. Board Status

```
sts = inp (BASE+0x2) ; /* Status */
```

Read (BASE+2H) Register provides the Status of the Board.

Table 3-8. Read (BASE+2H) Register Bit Field

Bit	Term	"=1" specifies	"=0" specifies	On Reset
B7	Not used.			0
B6	External input "UPD-IN" <Note-1>			0
B5	Not used.			0
B4	Not used.			0
B3	Interrupt request flag <Note-2>	Occurred	Not-Occurred	0
B2	Not used.			0
B1	Not used.			0
B0	Busy flag <Note-3>	Busy	Not-Busy	0

<Note-1>

Bit "**B6**" is the current state of external input "UPD-IN". See section 3-2 and 3-5 for the function of "UPD-IN".

"UPD-IN" is also available for general purpose digital input where you do not program as the update input.

<Note-2>

Bit "**B3**" shall be set by the specified edge of the external input "UPD-IN" that enabled as the interrupt input.

See section 3-6 for the details.

<Note-3>

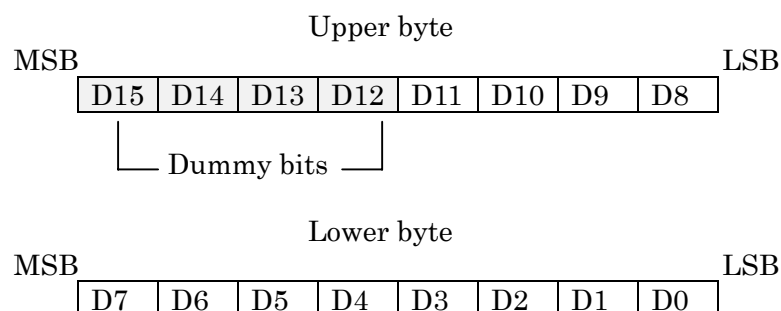
Bit "**B0**" shall be set while transferring the analog update data.

Wait until Bit "**B0**" return to "0" before writing the next analog update data.

3-9. Write DA-data

One 12-bits DA-data consists of upper 4-bits and lower 8-bits. They should be written as two byte data. Upper 4-bits of the upper byte are ignored as dummy.

The code of the data is straight-binary for uni-polar (0 to +10v) output range, or offset-binary for bi-polar (-10v to +10v) output range.



Individual Asynchronous Update.

Write lower byte first, then follow upper byte to any channel address, and latch of the DA-converter shall be updated at the timing of writing upper byte.

Simultaneous Synchronous Update.

Write DA-data from Channel-0 to N as same as individual immediate direct update, then finally, Write (BASE+0xB) Register as a simultaneous update command.

Prepare,

```
Rst = inp (BASE+0x7) ; /* Reset the Board, "Rst" is the board ID */
Outp (BASE+0x2, 0x0) ; /* set external control, see section 3-6. */
Outp (BASE+0x4, mode) ; /* Asynchronous or Synchronous, see section 3-5. */
Outp (BASE+0x5, rng) ; /* Analog Output Range, see section 3-7. */
```

Then,

```
Outp (BASE+0x8, ch0-L) ; /* Lower byte data for Channel-0 */
Outp (BASE+0x9, ch0-U) ; /* Upper byte data for Channel-0 */
Outp (BASE+0xA, ch1-L) ; /* Lower byte data for Channel-1 */
Outp (BASE+0xB, ch1-U) ; /* Upper byte data for Channel-1 */
Outp (BASE+0xC, ch2-L) ; /* Lower byte data for Channel-2 */
Outp (BASE+0xD, ch2-U) ; /* Upper byte data for Channel-2 */
Outp (BASE+0xE, ch3-L) ; /* Lower byte data for Channel-3 */
Outp (BASE+0xF, ch3-U) ; /* Upper byte data for Channel-3 */
```

In case for Simultaneous update mode,

Finally,

```
outp (BASE+0x7, upd) ; /* Simultaneous Update, "upd" is a dummy */
```

<Note> See section 3-2 for more information.

3-10. Master-Slave Operation

Synchronized Master-Slave operation is also available with multiple boards.

Master-board provides the update timing to the Slave-boards for synchronizing the update between them.

On-Board Hardware Configurations.

- (1) Set those Address by the switches SW1, SW2, and SW3 with differences against each other. See section 1-5 for details.
- (2) Analog Output Range is on your choice, any differences between them do not cause trouble.
- (3) Set interrupt level by the jumper JP-INT of Master-board if use. See section 3-6 for details.

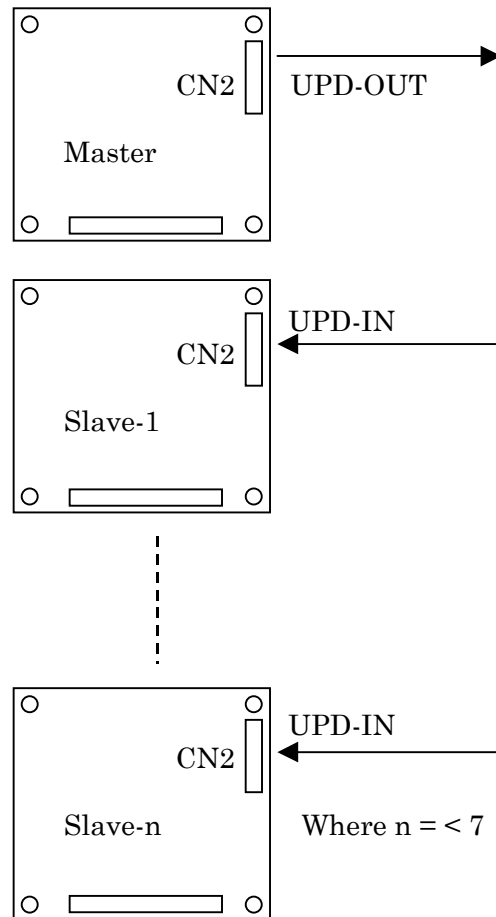
Board to Board Connections.

Update output (UPD-OUT) of Master must be connected to the external update input (UPD-IN) of the Slaves. Master can drive 7 Slaves directly. If more than 7 Slaves are needed, you can connect the Clock from 7th Slave to additional 7 Slaves as well as between Master and Slaves. See figure 3-10.

Software Flow.

- (1) Write DA-data into each address of the board.
- (2) Write (BASE+7H) Register as a synchronous update command for master slave operation as same as a simultaneous update operation in a board.

Figure 3-10. Master-Slave Connection



3-11. General Purpose Digital I/O

Din = inp (BASE+0x3) ; /* General Purpose Digital Inputs */
 outp (BASE+0x3, GPQ) ; /* General Purpose Digital Output */

Digital Input

Read (BASE+3H) Register specifies the 3bits current state of external TTL Inputs “D0-IN”, “D1-IN”, and “UPD-IN” which assigned on Connector “CN2”.
 See figure 1-7 of section 1-7.

Table 3-11A. Read (BASE+3H) Register Bit Field.

Bit	Input assignment	“=1” specifies	“=0” specifies
B7 B6 B5 B4 B3	Not used		
B2	“UPD-IN” as an External Update Input	High (or Open)	Low
B1	“D1-IN” as a General Purpose Digital Input	High (or Open)	Low
B0	“D0-IN” as a General Purpose Digital Input	High (or Open)	Low

Digital Output

Write (BASE+3H) Register specifies the 1bit assigned on Connector “CN2”.
 of General Purpose Digital Output which See Figure 1-7 of section 1-7.

Table 3-11B. Write (BASE+3H) Register Bit Field. / Where S-POL set to “N” /

Bit	Output assignment	“=1” specifies	“=0” specifies	On Reset
B7 B6 B5 B4 B3 B2 B1	Not used			0 0 0 0 0 0 0
B0	“Q0-OUT” as General Purpose Digital Output	Low	High	0

<Note-1>

Write (BASE+3H) Register is not cleared by Read (BASE+7H) Register as a Board-Reset Command, but cleared by the hardware reset or power-on process.

<Note-2>

Logical Polarity is set to Negative with setting the switch S-POL to “N” on shipping cause “Q0-OUT” to TTL high state at the hardware reset in power-on process.

Section 4. Maintenance and Appendix

4-1. Trouble Shootings

Reconfirm.

The QDA-724PC104 supplied by MICRO SCIENCE is fully calibrated and tested. If it doesn't work on your system, reconfirm following issues.

- (1) Check the I/O BASE address specified by the on-board switch SW1, SW2, and SW3. On the IBM PC/AT compatible system, the I/O address must be mapped between "0H" to "3FFH" or the image of this range except for the occupied address by the other devices or the peripherals.
- (2) Debug your software or applications. For example, if the Interrupt level is correct or if occupied by any other devices.
- (3) Be careful to input the signal at the Input of the External Digital Input "UPD-IN", "D0-IN", and "D1-IN". Applying the voltage of higher than +7v or lower than -0.5v to these HCT-type TTL level inputs shall cause permanent destruction of the front-ended devices. For example, Multi Wave Form Generator is that!

What's wrong?

Fill in and send (Letter, Fax, or Email) the Q&A form to MICRO SCIENCE where you didn't find anything wrong.

Although we will study about your system and answer by the letter what you should do, we don't write or debug application software.

Sorry, we won't answer with any language but Japanese on the phone. Please write us Japanese or English.

Replace the Board or Repair for free.

MICRO SCIENCE will replace or repair the Board for free which are after examination disclosed to the satisfaction of MICRO SCIENCE to be thus defective, for a period within one year of shipment. This warranty shall not apply which have been subject to misuse, negligence, or accident. See "Caution/Warranty" for details in page-4.

Repair the Board.

MICRO SCIENCE will repair, calibrate, or test the Board on request. These products should have to prepaid the transportation at MICRO SCIENCE. Be sure, give us the information with the products, maybe Q&A form is useful for the report.

Then user have to pay the proper cost in few weeks according to the bill after accept the returned products.

4-2. Calibration

QDA-724PC104 is supplied by MICRO SCIENCE fully calibrated and tested. However, before execute the user application and or at the chance of inspection for the system maintenance, you had better to calibrate the Board with the standard source.

Procedure.

- (1) Measure the voltage between “TP+” and “TPG” as the test point of reference output.
- (2) Trim the POT “TMG” to have +10.000 v sharp, and your QDA-724PC104 is calibrated within 0.058% of Full-Scale plus accuracy of the volt meter.

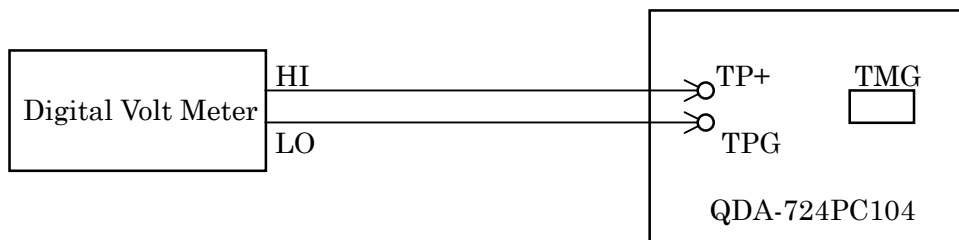
<Note-1>

This adjustment is only for the reference voltage of QDA-724PC104. You have no way that Offset and Gain trimming for individual analog output. The optimizing adjustment for particular channel cause decrease the accuracy of other channels.

<Note-2>

QDA-724PC104 is calibrated within 0.07% of Full-Scale accuracy at the factory of MICRO SCIENCE, though QDA-724PC104 has 0.004% of Full-Scale non-linearity, and 0.058% of Full-Scale differential accuracy among whole channels.

Figure 4-2. Measure between “TP+” and “TPG”



Q & A form (in English or Japanese)

To:
MICRO SCIENCE., Co. LTD
 Customer Support Div
 2-37-12, Nishiogi-kita,
 Suginami-ku,
 Tokyo, Japan

From:

Fax: +81-3-3301-5593
 Email: gas@microscience.co.jp

Fax:
 Email:

QDA-724PC104	serial # =	Purchase Date:
Preferences on- Board	SW1 =	JP-INT =
	SW2 =	S-POL =
	SW3 =	
Other Devices In the system	Product:	
	Occupied Resources: (I/O Address =), (Interrupt =)	
System Information	CPU:	
	OS :	
Software	Language:	
	Compiler:	

(Information)

<Note> MICR SCIENCE does not answer on phone with any language but Japanese.