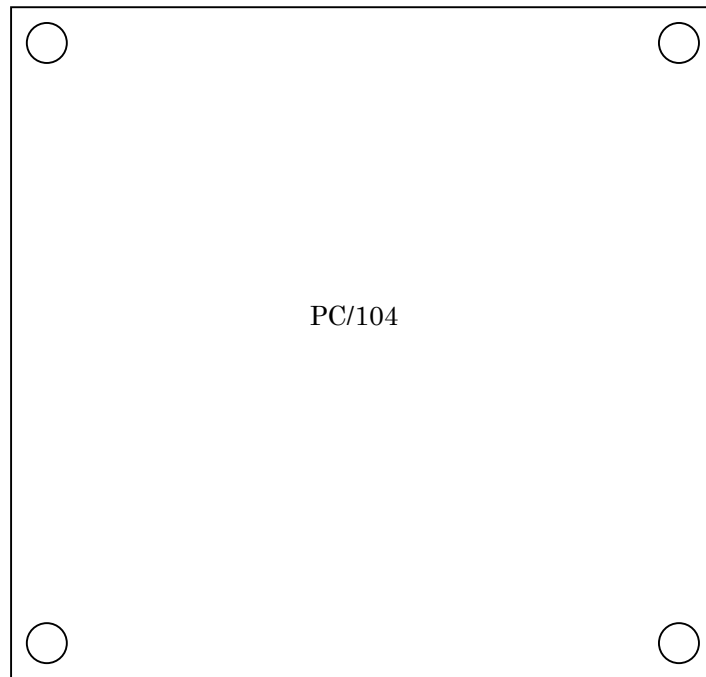


Real Solution for FA & LA



32bit Sampling Digital Output Board

**MDO-212PC104**

**User's Manual**

PC/104-BUS

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Mar 11, 2002

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## Caution

### Unpacking

This package contain a MDO-212PC104 board, and 4 pieces of 15mm spacer  
Upon receipt the package, visually inspect the board for missing or damaged materials. This product was shipped in perfect condition as it was new.  
Examine the package for physical damage. In the event of damage, save all packing materials and notify your courier to validate shipping claims.

### Anti-static discharge

The MDO-212PC104 contains components that are susceptible to static discharge, and should be handled with appropriate caution. The anti-static packing material protects components from being damaged by static discharge.  
Should the MDO-212PC104 board need to be returned for repair at a later date, it can be safely done by packing it in the original materials.

### Warranty

MICRO SCIENCE warrants that this product was manufactured free of defect in materials or workmanship under normal use and service as described in this User's Manual. Obligations under this warranty are limited to replacing or repairing at MICRO SCIENCE's option.  
Any said of products, at MICRO SCIENCE's factory or facility, should have to be prepaid transportation charges, and which are after examination disclosed to the satisfaction of MICRO SCIENCE to be thus defective, for a period within one year shipment.  
These provisions do not extend the original warranty period of any product which has either been repaired or replaced by MICRO SCIENCE.  
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This warranty shall not apply to any such products which have been repaired or altered except by MICRO SCIENCE or which have been subject to misuse, negligence, or accident.

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However, MICRO SCIENCE assumes no responsibility for errors or omissions. MICRO SCIENCE reserves the right to make changes to this manual without prior notification in accordance with the purpose of product support and or improvement.

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In this Agreement, a “FILE” shall mean a contiguous collection of machine-readable symbols, bytes, characters, or codes which may be used by the CPU on the user’s computer or processing equipment.

A “PROGRAM” is a file or related group of files which may be loaded and processed on the user’s computer or processing equipment to perform the functions.

A “SOFTWARE” shall mean one or more FILES or PROGRAMs.

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## Customer Product Support Policy

MICRO SCIENCE will answer the written questions ( including FAX, or Email) in Japanese or English from the registered user about this product.  
Send us the question form in this manual filled with the information.

We do not answer on phone with any language but Japanese.  
Although MICRO SCIENCE may offer advice, we will not design the user's application.

### Price List (# on Feb, 2002)

Items	Unit Price	Description
MDO-212PC104	\$ 330.00	32-bit Sampling Digital Output board for PC/104
User's Manual	\$10.00	Printed one. (PDF file is free for download from WEB)

# The product consists of a MDO-212PC104 board and 4 pieces of standoff.

**WEB :** [www.microscience.co.jp/eng/](http://www.microscience.co.jp/eng/)

#### **FIFO memory extend Option**

A standard MDO-212PC104 board have 2048 byte length FIFO buffer memory, at the first stage of the data stream.

We also provide more long FIFO memory on request.

Please add the code next to follow the product name as below.

**MDO-212PC104- 16KB** : for 16K byte length FIFO (Price: add \$100.00)

**MDO-212PC104- 2MB** : for 2M byte length FIFO (Price: add \$220.00)

**MDO-212PC104- 16MB** : for 16M byte length FIFO (Price: add \$340.00)

## Section 1. Introduction

### 1-1. Guide this Manual

This Manual contains a complete set of hardware and programming information for the MDO-212PC104 board, including configuration, installation, and I/O connection.

Section 1 contains the outline of functional descriptions and detail specifications, the installation, and setup procedure for the board.

Section 2 contains the detail of Input and Output functions.

Section 3 contains the digital output data sampling sequence and the post trigger operation.

Section 4 contains the trouble-shootings, and repair.

The last page is the request form for the Q and A.

### 1-2. Functional Specification

#### Digital Outputs

---

Number of Output	32-bits, 24-bits, 16-bits, or 8-bits parallel. (software selectable)
Output Level	TTL compatible, Isink=24mA.

#### Paced Update Mode (selectable on user program)

---

Update Rate	Up to 4MHz on Paced Update mode.
Paced Update	Digital Outputs are sampling synchronously with the Pacer Clock that start with the trigger.
Gated Update	In his mode, It works same as Paced Update, only in the period of software selected External Digital Trigger level.

#### Control Elements for Paced Update

---

Pacer Clock Source	Internal: 20MHz /accuracy:100ppm/, or External TTL input (= < 10MHz)
Pacer Clock (=Sampling Interval)	Divide the source by 32bit binary counter
Triggers	Software, Digital (External TTL Input): Falling or Rising edge, Level for Gated Update.
Buffer Memory	2K(=2048) byte FIFO type, Expandable to 16K, or 16M byte. (see Price List)

**General Purpose Digital I/O**

---

Input (74HCT-type TTL level)	3 External Inputs (Clock Source, Digital Trigger, Interrupt) are work for their own function with the program. If they have not programmed for the function, they work for a general purpose TTL level Input.
Output (CMOS level)	1 bit (latched output)

**System Configuration**

---

Bus Compatibility	PC/104 Bus All signals are driven or accepted by the C-MOS device. (74HCT type)
Board Address ###	Upper 12Bits: programmable by on-board switches. Lower 4Bits: on-board logic decoded for multiple I/O ports.
Interrupt ###	IRQ3,4,5,6,7,9

**I/O Connectors**

---

Digital Output	40pin FRC type (2.54mm pitch) x 2
Control Elements and General Purpose I/O	10pin FRC type (2.54mm pitch)

**Physical, Environmental**

---

Operating Temperature Range	0 to +55
Storage Temperature Range	-10 to +85
Relative Humidity	80% (Non-condensing)
Power Supply, Consumption	+5v 0.5 A



### 1-3. Functional Description

MDO-212PC104 is designed for multiple digital Output channels, can not only immediate update but also seamless non-stop paced update applications. The board updates the data up to 32-bits digital TTL level outputs. It is also available master-slave operation for multiple boards by the input and output of the clock.

The digital data update rate is up to 4MHz for 8-bits, 2MHz for 16-bits, 1.33MHz for 24-bits, and 1MHz for 32-bits simultaneous parallel outputs.

The paced method allows you to have each sampling process initiated at precise time intervals or synchronized with the external events.

The pacer clock period is software programmable by 32bit binary counter as a divide ratio to the source.

The clock source is also software selectable from internal 20MHz or external TTL input.

The software programmed trigger makes the pacer clock start or enable.

The variety of trigger allows the board to be adapted to a wide variety of applications. They are immediate on-software, External TTL input edge, or levels.

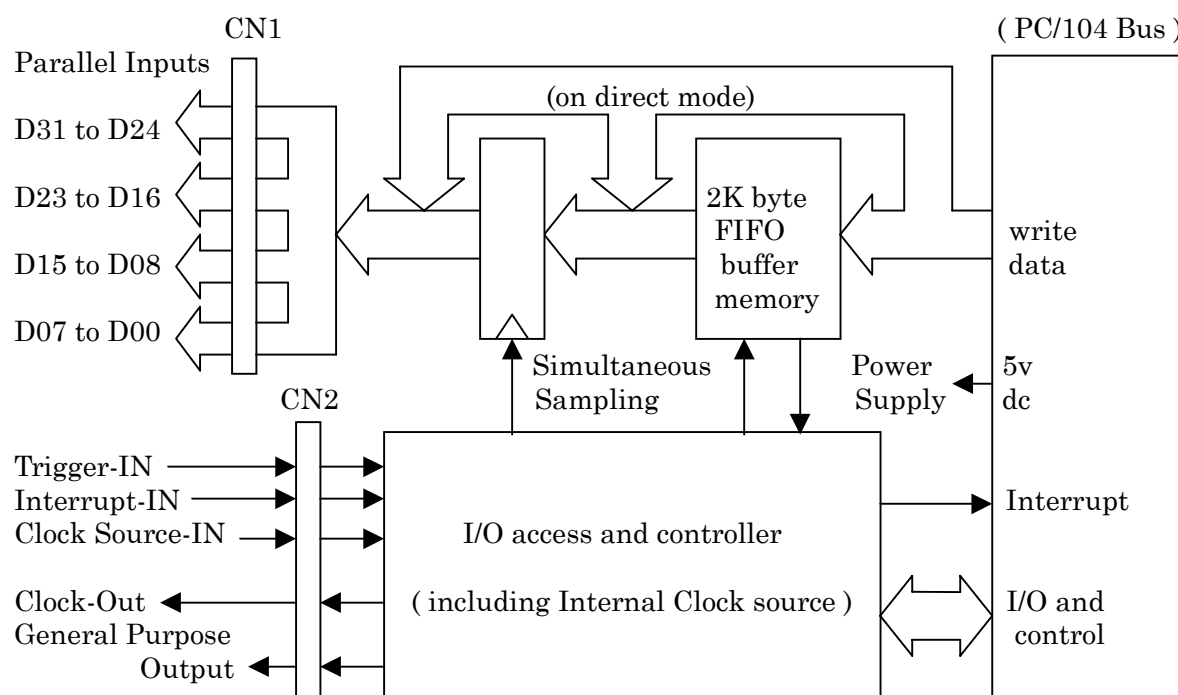
External TTL Trigger input level can be used for the gated update.

On-board FIFO type buffer memory allows the user asynchronous parallel-data write into the board. Not-Full or Half-Full state of the memory can not only usable for polled status write in, but also for Interrupt request.

Set the jumper-plug on the Interrupt level, if you use the function.

The base address of the board is programmable with the on-board switches.

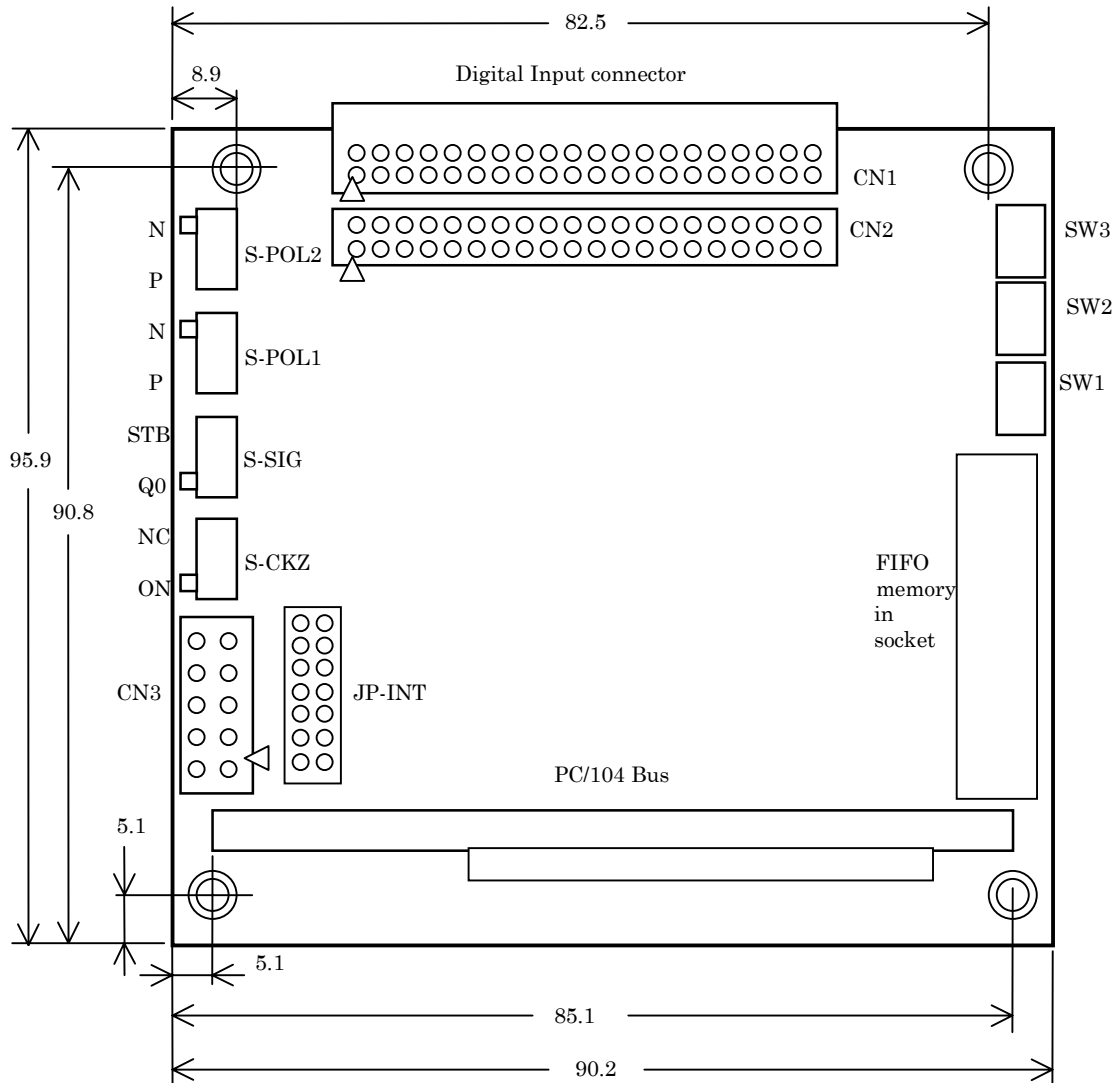
Figure 1-3. Functional Block Diagram



<Note> FIFO memory is Expandable to max.16M byte in option.

## 1-4. Layout of the board

Figure 1-4.



Unit: mm

At shipping, on-board programmable elements are set to < > position.

- # SW1, SW2, SW3: Program switch for Base Address of the board. <0,1,B> / see 1-5-1./
- # JP-INT : Select jumper-switch for Interrupt Level. <NC> / see 1-5-2./
- # S-POL2: Select switch for Polarity of 32-bits Digital Output. <N> / see 1-5-3./
- # S-POL1: Select switch for Polarity of General Purpose Output. <N> / see 1-5-3./
- # S-CKZ : Select switch for Clock Signal Terminator connection. <ON> / see 1-5-4./
- # S-SIG : Select switch for pin-9 of connector CN3. <Q0> / see 1-5-5./

- # CN1: Connector for Digital Input D16 to D31 (40pin, FRC) : contact from aside.
- # CN2: Connector for Digital Input D00 to D16 (40pin, FRC) : contact from above.
- # CN3: Connector for Digital Input and output (10pin, FRC) : contact from above.



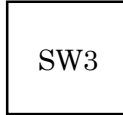
1-5. Settings on the board

1-5-1. BASE ADDRESS

MDO-212PC104 appears as a 16-byte block of registers within the host CPU's I/O address space. This address block must not conflict with other system I/O devices. You can program the on-board switches SW1, SW2, and SW3 as BASE ADDRESS of the board.

These hex-a-decimal defined switches are set to SW1=0, SW2=1, SW3=B at the factory of MICRO SCIENCE, that define the BASE ADDRESS to "01B0" hex. MDO-212PC104 occupies upper 16 byte address from the BASE. See section 3-3 for more information.

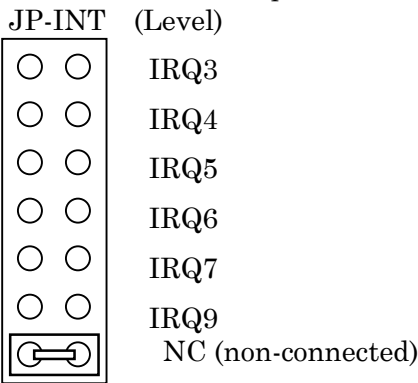
Figure 1-5A. Setting the BASE ADDRESS

Address Line →	AB15 to AB12	AB11 to AB08	AB07 to AB04	AB03 to AB00
On-board Hex-a-decimal → Switches				on-board logic decoded for multiple ports
Factory setting →	0	1	B	( F to 0 )

1-5-2. Interrupt Level

Hardware state of MDO-212PC104 can cause an interrupt request to the CPU. Select the interrupt level by the jumper-switch "JP-INT", and program Write (BASE+AH) register to enable the state. See section 3-13 for the details.

Figure 1-5. select the Interrupt Level.



1-5-3. Polarity of Digital Output

MDO-212PC104 has TTL level 32-bits sampling and 1-bit general purpose output. Select the logical polarity of the output by the switch "S-POL1" and "S-POL2" .

These switches are set to "N" at the factory of MICRO SCIENCE that defines the logical polarity to "Negative". You can also switch to "P" for "Positive".

1-5-4. Clock Input Termination

In case of using the External Clock Source Input "CLK-IN" that must be terminated with the resistor by set the on-board switch "S-CKZ" to "ON".

In case of Master-Slave operation, set the switch "S-CKZ" to "ON" at only one of the Slave board, and set to "NC" for the others including Master board.

1-5-5. pin-9 of connector CN3

Set "S-SIG" to "Q0" cause pin-9 of connector CN3 output specifies to general purpose output "GPQ-OUT", or set "S-SIG" to "STB"





















cause pin-9 of connector CN3 output specifies to strobe output "STB". See section 3-2 for detail of "STB".

## 1-6. Digital Output Connector

32-bits Parallel Digital Outputs are available on two 40-pin FRC-type male connector CN1 and CN2 on the board as illustrated in Figure 1-4.

The plug is also provided for general purpose, come with the board.

Figure 1-6. Digital Input Connector CN1 ,CN2 pin assignment

/Function/	Sign(CN1)	Sign(CN2)	pin assign	sign	/Function/
Digital output	Q0	Q16	1 	2	DG /Digital common/
	Q1	Q17	3 	4	DG
	Q2	Q18	5 	6	DG
	Q3	Q19	7 	8	DG
	Q4	Q20	9 	10	DG
	Q5	Q21	11 	12	DG
	Q6	Q22	13 	14	DG
	Q7	Q23	15 	16	DG
	Q8	Q24	17 	18	DG
	Q9	Q25	19 	20	DG
	Q10	Q26	21 	22	DG
	Q11	Q27	23 	24	DG
	Q12	Q28	25 	26	DG
	Q13	Q29	27 	28	DG
	Q14	Q30	29 	30	DG
	Q15	Q31	31 	32	DG
			33 	34	
			35 	36	
			37 	38	
			39 	40	

<Note.1> DGs are the Digital Common.

They are connected each other on the board.

<Note.2> All Output are TTL level. (74LS244)

<Note.3> Blank signed pins are not connected any where.

<Note.4> On-board bracket : Model = HIF3FC-40PA-2.54DSA / made by HIROSE /  
Plug : Model = HIF3BA-40DA-2.54R(11) / made by HIROSE /

## 1-7. Digital Input and Output Connector

Digital Inputs and Outputs are available on a 10-pin FRC-type male connector CN3 on the board as illustrated in Figure 1-7. They are External Clock Source Input, External Trigger Input, External Interrupt Input, Pacer Clock Output, and General Purpose latched Output.

All Inputs are 74HCT-type TTL level input, and pulled-up with 10K ohm resistor.

All outputs are also 74HCT-type CMOS level.

3 External Inputs should work for their own function with the program.

If they have not programmed for the function, they work for General Purpose Digital Input.

See section 3-2 for programming.

The plug is also provided for general purpose, come with the board.

Figure 1-7. Digital Input and Output Connector CN3 pin assignment

sign	Function	pin assign	sign /Function/
INT-IN	External Interrupt Input	1	DG /Digital common/
TRG-IN	External Digital Trigger Input	3	DG /Digital common/
CLK-IN	External Clock Source Input	5	DG /Digital common/
CLK-OUT	Pacer Clock Output	7	DG /Digital common/
GPQ-OUT <Note.4>	General Purpose Digital Output	9	DG /Digital common/

<Note.1> DGs are the Digital Common.

They are connected each other on the board.

<Note.3> On-board bracket : Model = HIF3FC-10PA-2.54DSA / made by HIROSE /

Plug : Model = HIF3BA-10DA-2.54R(11) / made by HIROSE /

<Note.4> pin-9 of the connector CN3 output is specified by the switch "S-SIG".

Set "S-SIG" to "Q0" cause that to general purpose output "GPQ-OUT", or

Set "S-SIG" to "STB" cause that to sampling strobe output "STB".

See section 3-17 for "GPQ-OUT".

See section 3-2 for "STB".

### 1-8. Options (Long FIFO Memory)

MDO-212PC104 has 2048 byte length FIFO buffer memory for asynchronous data write into the board.

On the typical application, it is enough capacity to have seamless data-update.

Although on the special application like a high performance multi-tasking system, long length FIFO memory may be expected. MICRO SCIENCE also provide that expansion to max.16M byte length for the convenience. See Price List for details.

## Section 2. Input and Output (details)

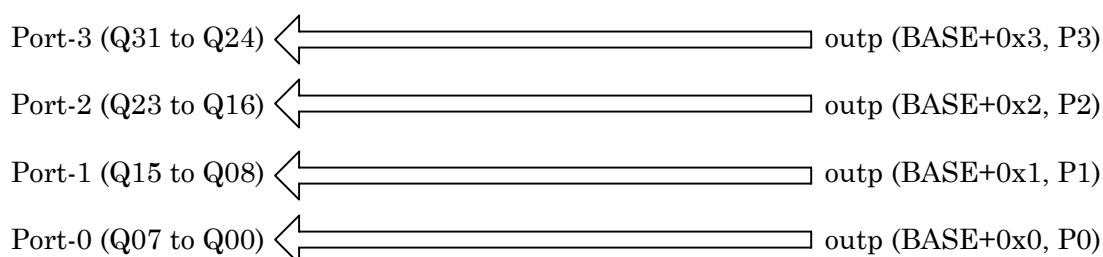
### 2-1. Digital Output configuration.

#### Direct Output.

MDO-212PC104 has 4-Registers as the direct outputs. Each of them consist of 8-bits. (All Output are TTL level.)

In this mode, every outputs are written directly, not through the FIFO memory. See section 3-15 for programming.

Figure 2-1A. Direct Output write operation.

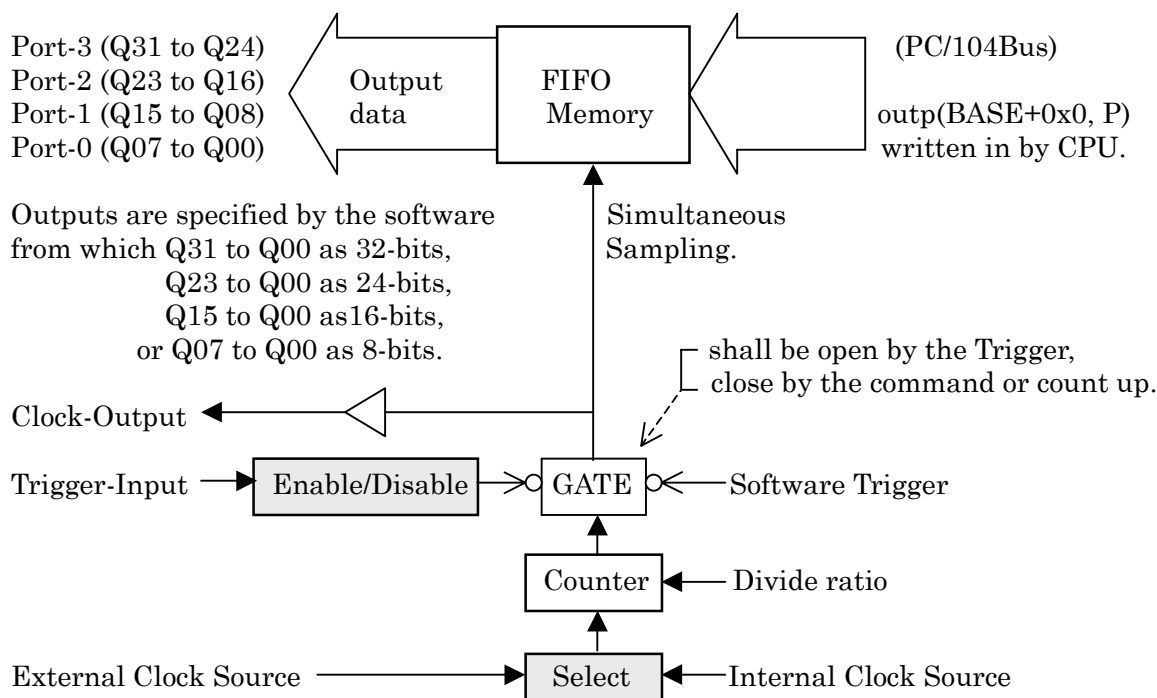


#### Paced Update.

Specified outputs are sampled with the Pacer Clock from the FIFO memory.

(All Output are TTL level.)  
See section 3-2 for programming.

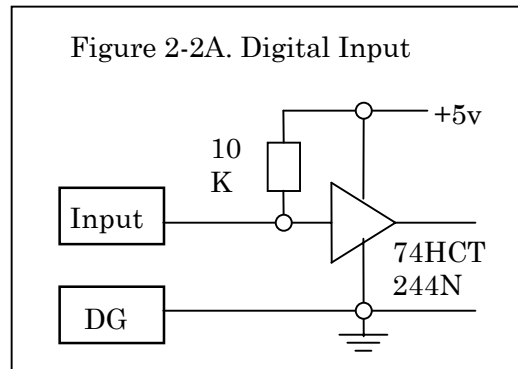
Figure 2-1B. Paced Update through the FIFO memory.



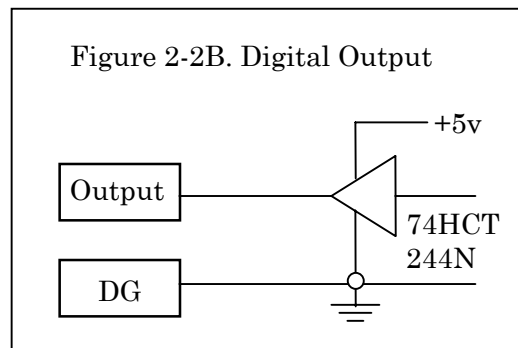
Where  shall be controlled with the software.

## 2-2. Control Input and Output

All control Inputs are 74HCT-type TTL level, and pulled-up to +5v with 10K ohm resistor.



All control Outputs are CMOS level.  
General Purpose Output is latched output, and you can select the logical polarity by on-board switch S-POL.  
MICRO SCIENCE set S-POL to "N" as Negative Logic, that cause the output to "CMOS-High" level at power-on reset.  
General Purpose Output does not clear by the software reset but clear by power-on hardware reset.





## Section 3. General Programming

### 3-1. General Programming Information

#### Handling

MDO-212PC104 appears to the host PC/104 bus CPU as a block of contiguous 16 hardware registers mapped within the I/O address space.

These registers control the operation of MDO-212PC104 as long as they are accessed using 16bit I/O addressing with each 8bit data transfers.

These registers include Reset-board, Outputs of Sampling object, Pacer Clock, Number of Sampling, Triggers, Start/Stop, Interrupt, Status, and General Purpose Digital I/O.

#### Operation

MDO-212PC104 does the buffering with on-board FIFO memory, and sampling output automatically.

It is necessary that the program provides the commands and parameters for the operation.

These are explained in order as follows.

( section 3-2 )

General sampling sequences in Direct Output mode and Paced Update mode.

( section 3-3 )

Trigger works as a start for Paced Update operation.

( section 3-4 )

Very useful on-board FIFO buffer memory for seamless Paced Update operation.

( section 3-5 to 3-17 )

The functions of each register. These are the elements for programming.

### 3-2. General Sampling Sequence

MDO-212PC104 has two kind of operation Mode. They are Direct Output mode, and Paced Update mode.  
See section 2-1 for Direct Output.

#### Paced Operation.

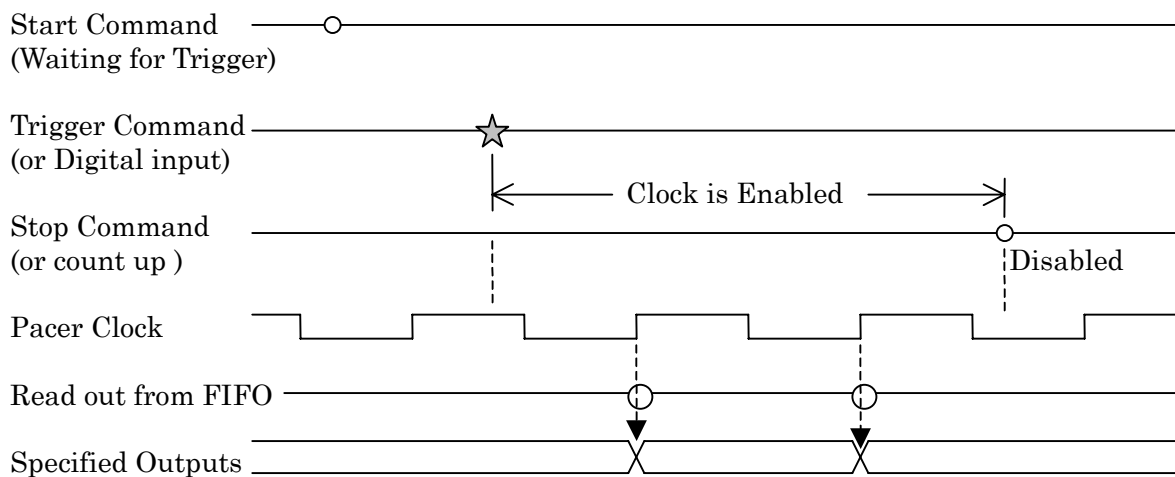
The data for Specified Outputs are read out from the FIFO memory then simultaneously Updated with the Pacer Clock for specified times or until Stop Command.

On-board FIFO memory works like a pipeline.

The data should be continuously read out from FIFO memory until it become Empty. Not-Full or Not-Half-Full state flag is useful for the trigger to write additional data into FIFO memory.

See section 3-4 for the detail of FIFO memory operation.

Figure 3-2A. Paced Operation process.



#### Procedure.

```

Rst = inp (BASE+0xF) ; /* Reset the Board, "Rst" is a dummy */
Outp (BASE+0x4, mode) ; /* set mode to paced update, see section 3-7. */
Outp (BASE+0x6, source) ; /* select Pacer Clock Source, see section 3-8. */
Outp (BASE+0x7, div-0) ; /* set Pacer Clock, see section 3-9. */
Outp (BASE+0x7, div-1) ;
Outp (BASE+0x7, div-2) ;
Outp (BASE+0x7, div-3) ;
Outp (BASE+0x8, num-0) ; /* set Times to Update, see section 3-10. */
Outp (BASE+0x8, num-1) ;
Outp (BASE+0x8, num-2) ;
Outp (BASE+0x8, num-3) ;
Outp (BASE+0x9, Trg) ; /* set Trigger mode, see section 3-11. */
Outp (BASE+0xA, intr) ; /* set interrupt source if use, see section 3-13. */
Outp (BASE+0xB, str) ; /* Start Paced operation, see section 3-12. */
Status-1 = inp (BASE+0xC) ; /* Get Status-1, see section 3-14. */
Status-2 = inp (BASE+0xD) ; /* Get Status-2, see section 3-14. */

/* To be written additional data into FIFO memory, see section 3-15 */

Outp (BASE+0xB, stp) ; /* Stop Paced operation, see section 3-12 */

```

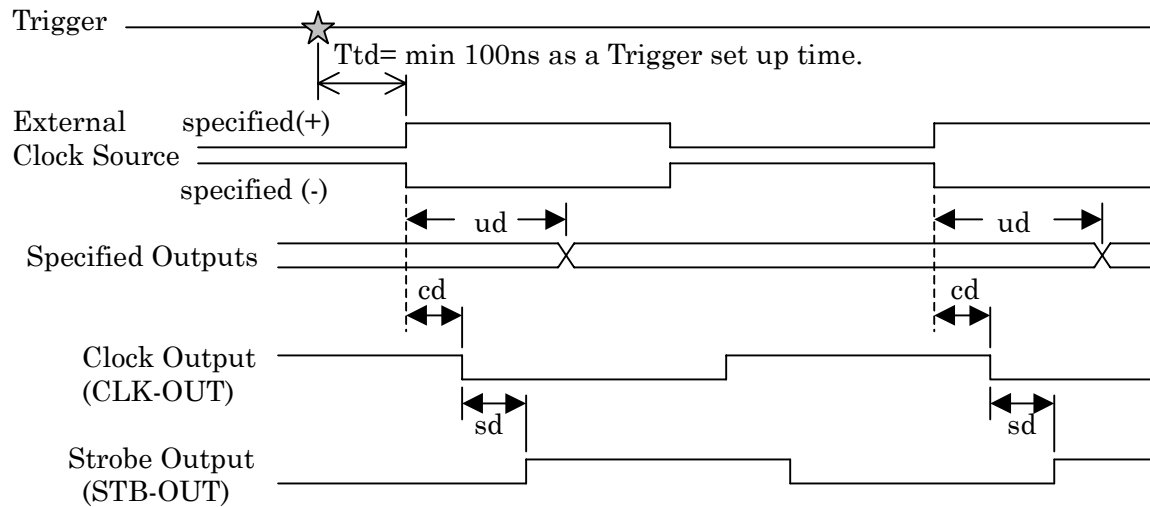
**3-2-1. Paced operation by divided Internal Clock Source.**

Sampling shall be started after 100ns of Trigger.  
Timing is similar as using External Clock Source  
illustrated in Figure 3-3C.

**3-2-2. Paced operation by non-divided External Clock Source.**

Sampling shall be started after 100ns of Trigger.  
Figure 3-2B shows the timing requirements between  
Non-divided External Clock Source and Specified Output data.

Figure 3-2B. Paced operation by non-divided External Clock Source.



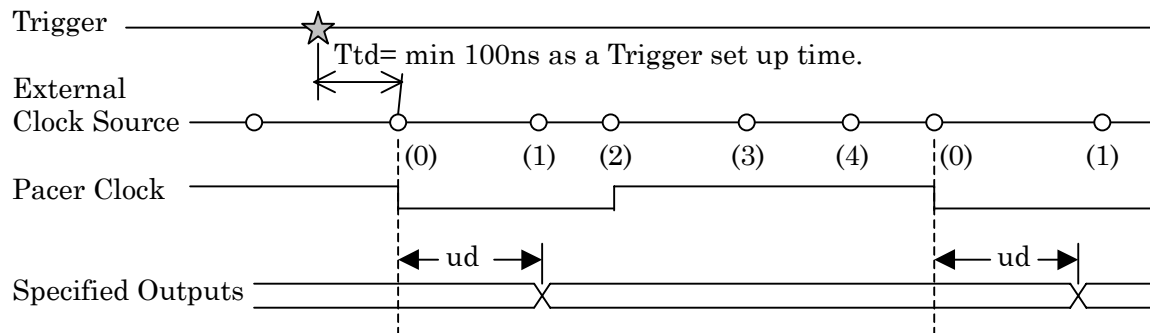
Where output delay "ud" = 1050ns for 32-bits simultaneous update.  
= 800ns for 24-bits simultaneous update.  
= 550ns for 16-bits simultaneous update.  
= 300ns for 8-bits simultaneous update.

Clock output delay "cd" = max 100ns,  
Clock output to Strobe output delay "sd" = 2 micro-second.

**3-2-3. Paced operation by divided External Clock Source.**

Sampling shall be started after 100ns of Trigger.  
Figure 3-2C shows the timing requirements between  
External Clock Source and specified Outputs.

Figure 3-2C. Paced operation by 1/5 divided External Clock Source.



Clock Output and Strobe Output are same as Figure 3-2B.

### 3-3. Variety of Triggers

The software selected trigger makes the Pacer Clock start or enable.

The variety of triggers allow the board to be adapted to a wide range of applications as follows.

See section 3-11 for the programming.

#### Software Trigger.

You can insert the Software Trigger Command as a immediate start for the Pacer Clock at any time or any point of the application software process.

#### External Digital Edge Trigger.

When External Digital Edge Trigger is enabled, rising or falling edge of External TTL level input “TRG-IN” makes the Pacer Clock start.

Figure 3-3A shows the operation, in which specified as a rising edge of “TRG-IN” for trigger is illustrated at upper side, and a falling edge is at lower side. They are also software selectable as a polarity of “+” or “-”.

#### External Digital Level Trigger.

External TTL level input “TRG-IN” can also be useful for the Gated Update that enable the Pacer Clock as long as the software selectable valid level.

Figure 3-3B shows the work of “TRG-IN” in which “valid level=High” for Gate-On is illustrated at upper side, and “valid level=Low” is at lower side.

Note that another Gated Update shall be executed if another “valid level” come as long as Digital Level Trigger is enabled.

Figure 3-3A.  
External Digital Edge Trigger

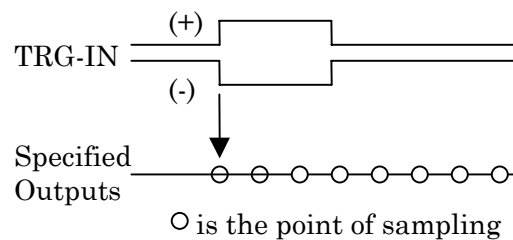
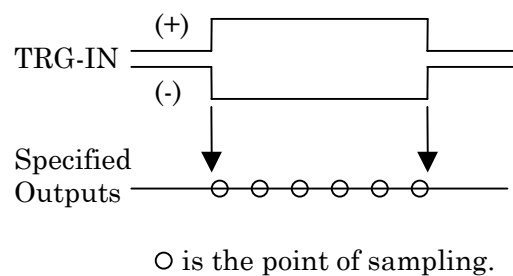


Figure 3-3B.  
External Digital Gated Update



### 3-4. On-Board FIFO Memory

On-Board FIFO buffer memory allows the program asynchronous data write in. The Program is always free from taking care of the hardware timing in data write in process while sampling process is being executed on the board.

MDO-212PC104 provides “Not-Full”, “Not-Half-Full”, and “Data-Lost” flag as the FIFO memory status.

In any time, the program can not only read the Flags for polled method of data write in, but also use them as the trigger for interrupt operation.

Figure 3-4A shows how the FIFO memory works on the board.

The standard model of MDO-212PC104 has 2048 byte of data capacity that is enough for many applications.

When the Pacer Clock read the data out from the FIFO memory, un-occupied area shall be expanded up to the capacity. This feature is very useful when the program need to write the data while sampling process is being executed and or need the unlimited acquisition.

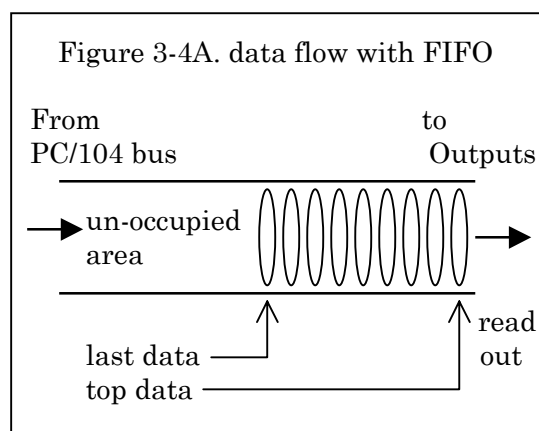


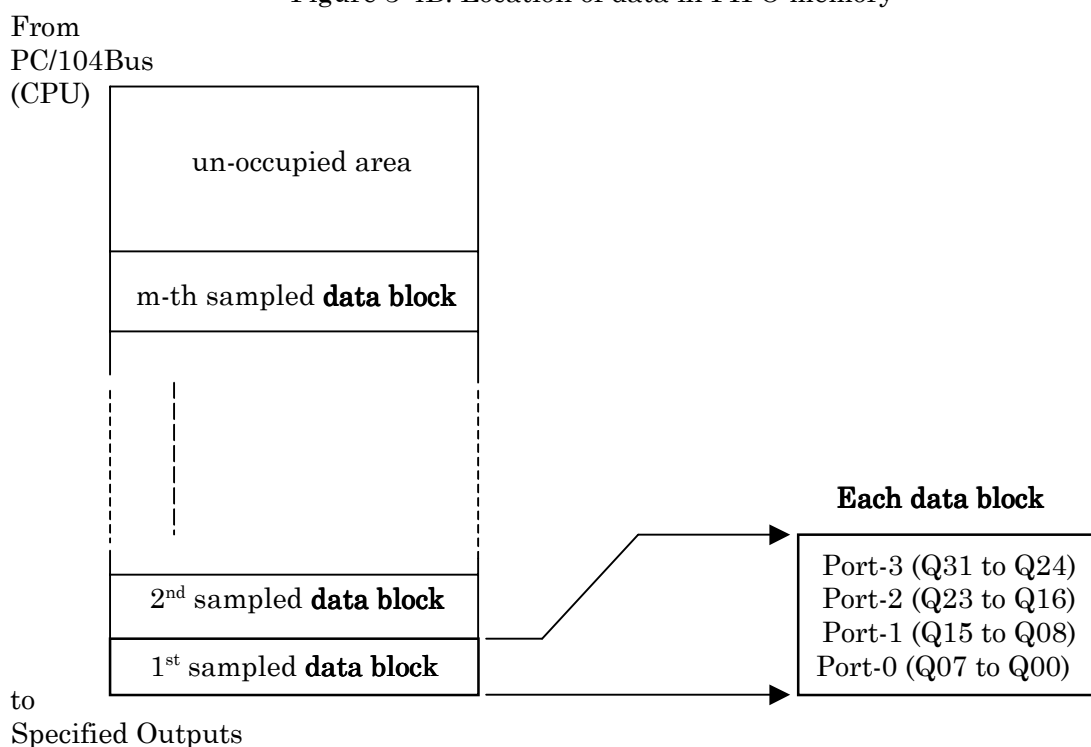
Table 3-4. Status Flag of FIFO memory

item	status
Not-Full	Acceptable one or more.
Not-Half-Full	Occupied greater than half of the capacity.
Data Lost	Borrow was happened.

It is possible to expand the capacity of FIFO memory by replace the device.

16K byte, 2M byte, or 16M byte is available at the purchase order in option.

Figure 3-4B. Location of data in FIFO memory





### 3-5. I/O Register Memory Map

MDO-212PC104 appears as a 16-byte block of registers within the host CPU's I/O address space. This address block must not conflict with other system I/O devices.

You can program the on-board switches SW1, SW2, and SW3 as BASE ADDRESS of the board.

These hex-a-decimal defined switches are set to SW1=0, SW2=1, SW3=B at the factory of MICRO SCIENCE, that specify the BASE ADDRESS to "01B0" hex.

MDO-212PC104 occupies upper 16 byte address from the BASE.

See figure 1-4 for the location of the board.

Figure 1-5A. Setting the BASE ADDRESS

Address Line →	AB15 to AB12	AB11 to AB08	AB07 to AB04	AB03 to AB00
On-board Hex-a-decimal Switches →	SW1	SW2	SW3	on-board logic decoded for multiple ports
Factory setting →	0	1	B	( F to 0 )

Table 3-5. MDO-212PC104 Register Assignment. (All the port consist of 8bit.)

I/O Address	Direction	Description	Refer to
BASE +FH	Read	Reset Board, and get ID.	Section 3-6
	Write		
BASE +EH	Read	External Control Elements Input state.	Section 3-17
	Write	General Purpose Digital Output. (latched)	
BASE +DH	Read	2ndary Status.	Section 3-14
	Write	Clear 2ndary Status.	
BASE +CH	Read	Primary Status.	
	Write	Clear Primary Status.	
BASE +BH	Read	Simultaneous Manual Output	Section 3-15
	Write	Start or Stop for Paced operation	Section 3-12
BASE +AH	Read		Section 3-13
	Write	Interrupt Source or State.	
BASE +9H	Read		Section 3-11
	Write	Trigger Source and Mode	
BASE +8H	Read	Paced Operation Counter.	Section 3-10
	Write		
BASE +7H	Read		Section 3-9
	Write	Divide Ratio to the Pacer Clock Source.	
BASE +6H	Read		Section 3-8
	Write	Pacer Clock Source.	
BASE +5H	Read		
	Write		
BASE +4H	Read		Section 3-7
	Write	Mode and Bit width of Output.	
BASE +3H	Read	/ Write Port-3 direct./	Section 3-15
	Write		
BASE +2H	Read	/ Write Port-2 direct./	Section 3-15
	Write		
BASE +1H	Read	/ Write Port-1 direct./	Section 3-15
	Write		
BASE +0H	Read	Write data into FIFO, or / Write Port-0 direct./	Section 3-15
	Write		

## 3-6. Reset the Board, and get ID

```
rst = inp (BASE+0xF) ; /* Reset the Board */
```

Read (BASE+FH) Register cause the board reset.

All registers of the board must be initialized except for the last values of General Purpose Digital Output described in section 3-17.

The paced operation process shall be broken, and previous data in the FIFO memory must be lost.

Where “rst” is the ID that depend on the board, “1BH” for MDO-212PC104.

Table 3-6. Read (BASE+FH) Register Bit Field.

Bit	Description
B7	1BH is the ID for MDO-212PC104.
B6	
B5	
B4	
B3	
B2	
B1	
B0	



## 3-7. Output Mode, Output Bit width

```
outp (BASE+0x4, mc) ; /* Mode and Data width */
```

Write (BASE+4H) Register specifies the Mode and bit width for Outputs.

## &lt;Note-1&gt;

Specified bits width data shall be read out from FIFO memory and update the Outputs with the Pacer Clock in Paced Update mode.

## &lt;Note-2&gt;

Outputs should be updated directly with the write command in Direct Input mode. Update timing is specified by the Bit “B5” on Direct Output mode.

Table 3-7A. Write (BASE+4H) Register Bit Field.

Bit	Term	“=1” specifies	“=0” specifies	on Reset
B7 B6	Not used.			0 0
B5	Timing on Direct Output mode.<Note-2>	Simultaneous	Individual	0
B4	Output Mode	Paced	Direct	0
B3 B2	Not used.			0 0
B1 B0	Output Bit width of each Sampling on Paced Update mode. <Note-1>	See Table 3-7B		0 0

Table 3-7B. Outputs for Paced Update

B1	B0	Output data Bit width	Outputs
1	1	32	Q31 to Q00
1	0	24	Q23 to Q00
0	1	16	Q15 to Q00
0	0	8	Q07 to Q00

Table 3-7C

B5	B4	Operation Mode
1	1	Paced Update <Note-3>
1	0	Simultaneous Direct Output
0	1	Paced Update <Note-3>
0	0	Individual Direct Output

<Note-3> Output timing is Simultaneous on Paced Update mode.

## 3-8. Pacer Clock Source Selection

outp (BASE+0x6, cks) ; /\* Clock Source \*/

Write (BASE+6H) Register specifies the Pacer Clock Source that should be divided to generate the Pacer Clock.

Table 3-8 shows the structure of the bit field. The bit “B4” select the Pacer Clock Source either Internal or External of the board.

The bit “B7” select the valid edge of the External Clock Source.

Where, External Clock Source Input “CLK-IN” must be TTL level, and the frequency is less than 10MHz.

Internal Clock Source is 20MHz.

Table 3-8. Write (BASE+6H) Register Bit Field.

Bit	Term	=”1” specifies	=”0” specifies	on Reset
B7	Select the valid edge of “CLK-IN”	Rising edge (+)	falling edge (-)	0
B6 B5	Not used			0 0
B4	Select the Pacer Clock Source	External “CLK-IN” (less than 10MHz)	Internal (20MHz)	0
B3 B2 B1 B0	Not used			0 0 0 0

<Note>

External Clock Source must be less than 10MHz,  
and both state of the level must be longer than  
45 ns.

## 3-9. Divide Ratio to Pacer Clock Source

outp (BASE+0x7, div0) ; /\* 1<sup>st</sup> data = Least significant byte of divide ratio \*/  
 outp (BASE+0x7, div1) ; /\* 2<sup>nd</sup> data = 3<sup>rd</sup> significant byte of divide ratio \*/  
 outp (BASE+0x7, div2) ; /\* 3<sup>rd</sup> data = 2<sup>nd</sup> significant byte of divide ratio \*/  
 outp (BASE+0x7, div3) ; /\* 4<sup>th</sup> data = Most significant byte of divide ratio \*/

Write (BASE+7H) Register specifies the divide ratio to the Pacer Clock Source that specifies the Pacer Clock.  
 Single 32-bit binary counter must be written as 4-byte data in order as describe above.

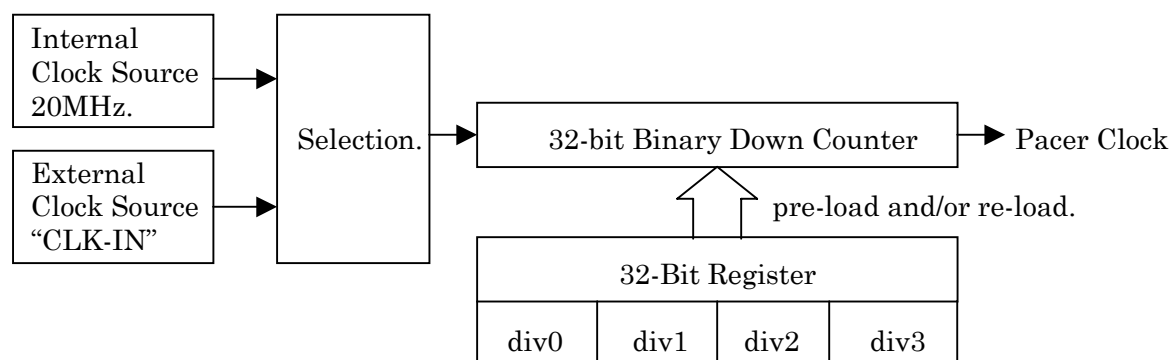
They are held in the same bit-wide registers and automatically re-load the counter at decrease to “0” by down-counting as a divider.

Figure 3-9 shows the configuration of generating Pacer Clock.

Table 3-9. Write (BASE+7H) Register Bit Field.

Bit	1 <sup>st</sup> data (div0)	2 <sup>nd</sup> data (div1)	3 <sup>rd</sup> data (div2)	4 <sup>th</sup> data (div3)	on Reset
B7	Least significant byte of divide ratio.	3 <sup>rd</sup> significant byte of divide ratio.	2 <sup>nd</sup> significant byte of divide ratio.	Most Significant byte of divide ratio.	0
B6					0
B5					0
B4					0
B3					0
B2					0
B1					0
B0					0

Figure 3-9. Configuration of generating Pacer Clock.



### 3-10. Paced Operation Counter

The number of sampling should be specified with the counter on Limited Paced operation mode. Other hand, this counter does not work on Un-Limited Paced operation mode. See section 3-12 for details.

#### (1) on Limited Paced Non-Cycle Update mode

```

outp (BASE+0x8, num0) ; /* 1st data = Least Significant byte */
outp (BASE+0x8, num1) ; /* 2nd data = 3rd Significant byte */
outp (BASE+0x8, num2) ; /* 3rd data = 2nd Significant byte */
outp (BASE+0x8, num3) ; /* 4th data = Most Significant byte */

```

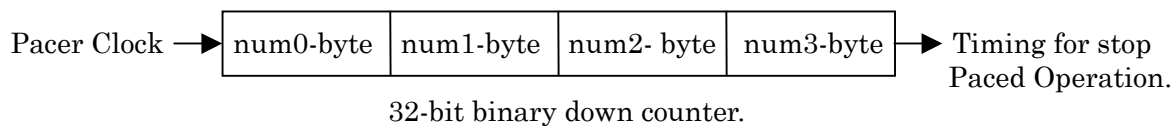
Write (BASE+8H) Register specifies the Number of update with the Pacer Clock. 32-bit binary pre-settable down counter must be written as 4-byte data in order as described above.

This Paced Operation Counter shall being count down by the Pacer Clock until decreased to “0”. Figure 3-10A shows the configuration of Paced Operation Counter.

Table 3-10A. Write (BASE+8H) Register Bit Field.

Bit	1 <sup>st</sup> data (num0)	2 <sup>nd</sup> data (num1)	3 <sup>rd</sup> data (num2)	4 <sup>th</sup> data (num3)	on Reset
B7	Least significant byte.	3 <sup>rd</sup> significant byte.	2 <sup>nd</sup> significant byte.	Most Significant byte.	0
B6					0
B5					0
B4					0
B3					0
B2					0
B1					0
B0					0

Figure 3-10A. Paced Operation Counter.



The program can also read out the counter as a rest of the sampling.

This 32-bit binary counter must be read as 4-byte data in order as described below.

#### Read out

```

Num0 = inp (BASE+0x8) ; /* 1st data = Least Significant byte */
Num1 = inp (BASE+0x8) ; /* 2nd data = 3rd Significant byte */
Num2 = inp (BASE+0x8) ; /* 3rd data = 2nd Significant byte */
Num3 = inp (BASE+0x8) ; /* 4th data = Most Significant byte */

```

## (2) on Limited Paced Cycle Update mode

```

outp (BASE+0x8, pnt0) ; /* 1st data = Lower byte of number of point */
outp (BASE+0x8, pnt1) ; /* 2nd data = Upper byte of number of point */
outp (BASE+0x8, tms0) ; /* 3rd data = Lower byte of repeat times */
outp (BASE+0x8, tms1) ; /* 4th data = Upper byte of repeat times */

```

Write (BASE+8H) Register specifies the Number of Update with the Pacer Clock. 32-bit binary pre-settable down counter must be written as 4-byte data in order as described above.

Digital pattern cycle data that consists of the “number of point” should be written in the on-board FIFO memory before start Paced Update operation.

Point Counter shall being count down to “0”, and re-load then count down to “0” with the Pacer Clock repeat until Times Counter decrease to “0”

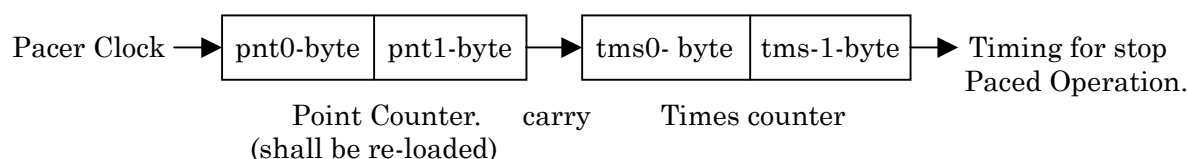
Times Counter shall being count down decreased to “0” by the carry of Point Counter.

Figure 3-10B shows the configuration of Paced Operation Counter in Cycle mode.

Table 3-10B. Write (BASE+8H) Register Bit Field on **Cycle mode**.

Bit	1 <sup>st</sup> data (pnt0)	2 <sup>nd</sup> data (pnt1)	3 <sup>rd</sup> data (tms0)	4 <sup>th</sup> data (tms1)	on Reset
B7					0
B6					0
B5					0
B4	Lower byte of number of point in one cycle.	Upper byte of number of point in one cycle.	Lower byte of repeat times for the cycle data.	Upper byte of repeat times for the cycle data.	0
B3					0
B2					0
B1					0
B0					0

Figure 3-10B. Paced Operation Counter on **Cycle mode**.



The program can also read out the Paced Operation Counter as a rest of the Updates. This 32-bit binary counter must be read as 4-byte data in order as described below.

“**Rest point**” is the rest number of point in current cycle.

“**Rest times**” is the rest number of times to be repeated the cycle.

#### Read out

```

Pnt0 = inp (BASE+0x8) ; /* 1st data = Lower byte of Rest point */
Pnt1 = inp (BASE+0x8) ; /* 2nd data = Upper byte of Rest point */
Tms0 = inp (BASE+0x8) ; /* 3rd data = Lower byte of Rest times */
Tms1 = inp (BASE+0x8) ; /* 4th data = Upper byte of Rest times */

```

## 3-11. Trigger Source and Mode

outp (BASE+0x9, tgm) ; /\* Trigger Source and Mode \*/

Write (BASE+9H) Register specifies the Trigger Mode, Source, and Polarity for the Paced operation.  
 Bit “B3” specifies the Digital Trigger Mode.  
 Bit “B4” specifies the Polarity of the Digital Trigger.

Bit “B6” specifies to enable or disable the Digital Trigger.  
 Bit “B7” specifies to enable or disable the Software Trigger.

Table 3-11A. Write (BASE+9H) Register Bit Field.

Bit	Term	“=1” specifies	“=0” specifies	on Reset
B7	Software Trigger.	Enable	Disable	0
B6	External Digital Trigger.	Enable	Disable	0
B5	Not used.			0
B4	Polarity of Digital Trigger.	+ (or Rising Edge)	- (or Falling Edge)	0
B3	Digital Trigger Mode	Edge	Level	0
B2	Not used.			0
B1				0
B0				0

## &lt;On and OFF the Paced operation&gt;

Start Command that specified in the next section 3-12 cause MDO-212PC104 into waiting for Trigger state, then Paced operation shall be started on detecting any Trigger that enabled, and stopped on the counter decrease to “0” on Limited Paced operation Mode.  
 Stop Command that specified in the next section 3-12 also cause to stop the Paced operation in any mode.

## &lt;Multi Trigger Source&gt;

Because both Trigger Sources are enabled or disabled individually, they work like the switches connected in parallel.

## &lt;Delay to Start&gt;

The delay time to start Paced operation with the Internal Clock Source from detect the Trigger is specified as follows.  
 On Software Trigger; 150ns (max),  
 On External Digital Trigger ; 180ns (max),  
 Other hand with the External Clock Source, plus 1 Clock Source Period to that value.

## &lt;Example&gt;

The procedure of Start Paced operation with the software Trigger is follows.

(1)

Write (BASE+9H) Register to Bit “B7”=1, then Write (BASE+BH) as a Start Command.

or(2)

Write (BASE+BH) as a waiting for Trigger Start Command, then Write (BASE+9H) Register to Bit “B7”=1 as a software immediate Trigger.

## &lt;Gated operation&gt;

External Digital Level Trigger works as a Gated operation that enabled by  
 Write (BASE+9H) Register to Bit “B6”=1, “B3”=0, and specify the Polarity with “B4”.  
 Paced operation shall be executed among the specified Level.

----- How the Trigger works for Paced operation -----

Specified Trigger operate with the Start Command for the post trigger Paced operation as illustrated in Figure 3-11A,B,C. Although these are illustrated as after Start Command, it is also valid that specify the Trigger before Start Command.

Where ▼ is the start-timing, ▽ is the stop-timing for Paced operation.

Paced operation shall be stopped by Stop Command or the counter decrease to "0" on the Limited mode.

Figure 3-11A. With the Software Trigger.

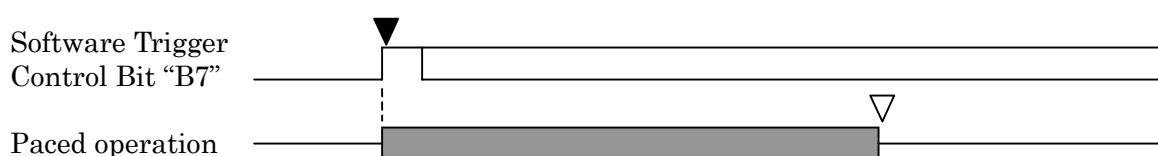
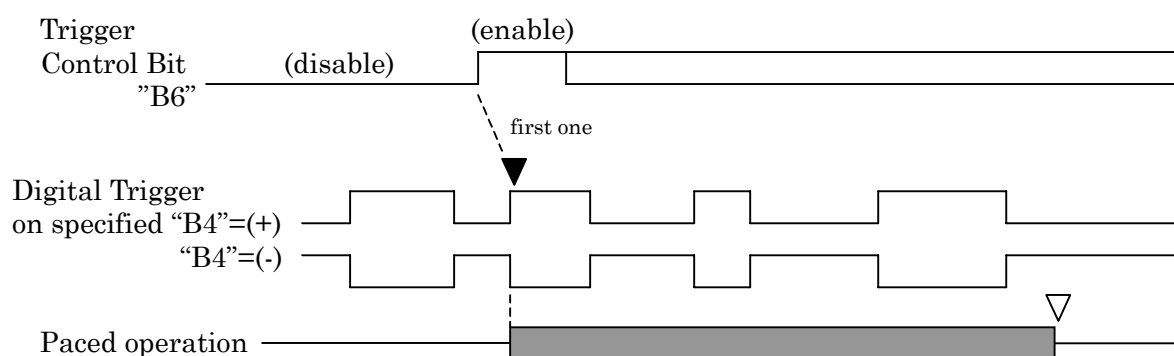


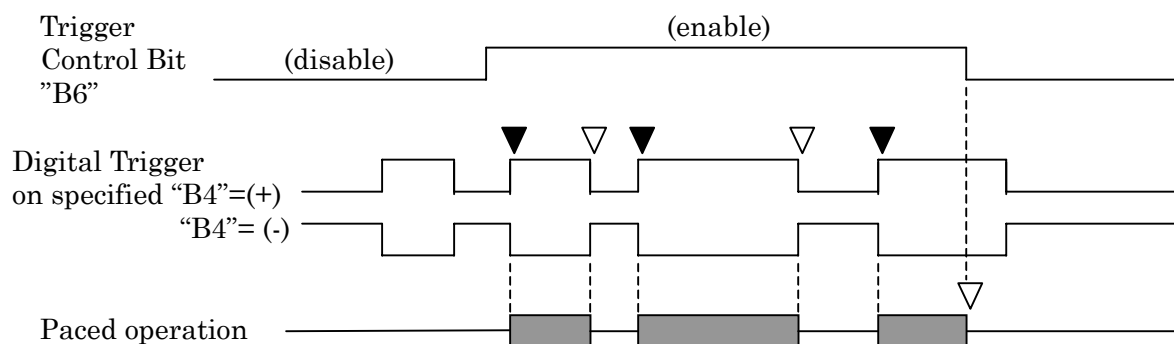
Figure 3-11B. With the Digital Edge Trigger.



<Note> After Enable and Start Command, the first valid Edge of "TRG-IN" is the Trigger.

Trigger Mode specify Bits must be set to "B3"=1 as a edge mode.

Figure 3-11C. With the Digital Level Trigger.



<Note> Trigger Mode specify Bits must be set to "B3"=0 as a level mode.

## 3-12. Start / Stop Paced operation

out (BASE+0xB, str) ; /\* Control the Paced Operation \*/

Write (BASE+BH) Register specifies the Paced operation Mode, and ON/OFF control.

Bit “**B7**” specifies the Paced operation whether Paced Update or only Pacer Clock run.

Bit “**B1**” specifies the Paced operation whether Un-Limited run until “Stop” or Limited run with the counter that is specified in section 3-10.

Bit “**B0**” controls Start and Stop the Paced operation.

Where “Start” means “waiting for Trigger” that is a post Trigger operation.

MDO-212PC104 is waiting for the Trigger to start the Paced operation by set “B0”=1, and shall be stopped by set “B0”=0.

Table 3-12A. Write (BASE+BH) Register Bit Field.

Bit	Term	“=1” specifies	“=0” specifies	on Reset
B7	Paced Operation	Pacer Clock only	Paced Update	0
B6	Not used			0
B5				0
B4				0
B3				0
B2				0
B1	Limited / Un-Limited operation.	Limited by counter	Endless	0
B0	Start / Stop Command	Start	Stop	0

(1) **Un-Limited run.**

This Command cause MDO-212PC104 into waiting for Trigger to start Un-Limited Paced operation that shall run until put “Stop” Command.

(2) **Limited run.**

This Command cause MDO-212PC104 into waiting for Trigger to start Limited Paced operation that shall run until count down to “0” of the counter or put “Stop” Command.

(3) **Un-Limited run only Pacer Clock.**

This Command cause MDO-212PC104 into waiting for Trigger to start Un-Limited run only Pacer Clock until put “Stop” Command.

(4) **Limited run only Pacer Clock.**

This Command cause MDO-212PC104 into waiting for Trigger to start Limited run only Pacer Clock until count down to “0” of the counter or put “Stop” Command.

<Note> **Re-Start.**

“Stop” command must be put before re-start Paced operation in case of stopped by the counter.

Table 3-12B. Bit pattern to control the Paced Operation.

B7	B1	B0	(start on trigger) Operation
1	1	1	Pacer Clock only, Limited run until “counter”=0, or “Stop” command.
1	1	0	Stop
1	0	1	Pacer Clock only, Un-Limited run until “Stop” command.
1	0	0	Stop
0	1	1	Limited Paced Update until “counter”=0, or “Stop” command.
0	1	0	Stop
0	0	1	Un-Limited Paced Update until “Stop” command.
0	0	0	Stop



## 3-13. Interrupt Source Selection

```
outp (BASE+0xA, isd) ; /* Interrupt Source */
```

Write (BASE+AH) Register specifies enable or disable individual Interrupt Source. Hardware state in the MDO-212PC104 that is enabled shall cause an interrupt request to the host CPU.

Interrupt request may be used to synchronize the transfer of data into MDO-212PC104 or something.

Interrupt Level is selected by the jumper switch “JP-INT” illustrated in Figure 1-5B.

Table 3-13A. Select the Interrupt Level.

“JP-INT”	Level
IRQ 3	3
IRQ 4	4
IRQ 5	5
IRQ 6	6
IRQ 7	7
IRQ 9	9
NC	Non-use

Table 3-13B. Write (BASE+AH) Register Bit Field

Bit	Interrupt Timing	“=0” specifies	“=0” specifies	On Reset
B7	Valid edge of Digital Input “INT-IN”	+ (rising edge)	- (falling edge)	0
B6	“Half-Full” state of FIFO memory	Enable	Disable	0
B5	“Not-Full” state of FIFO memory	Enable	Disable	0
B4	The End of the Paced operation	Enable	Disable	0
B3	The End of each Sampling scan.	Enable	Disable	0
B2	Detected the Trigger	Enable	Disable	0
B1	Digital Input “INT-IN”	Enable	Disable	0
B0	Initial edge of every Pacer Clock	Enable	Disable	0

Bit “**B7**” specify the valid edge of Digital Input “INT-IN” If it enabled.

Bit “**B6 to B0**” specify that enable or disable of each Interrupt Source.

Bit “**B4**” specify that enable or disable to interrupt by the counter decrease to “0” on Limited Paced Operation. Note, Stop Command doesn’t work for the Interrupt.

Bit “**B3**” control the interrupt source of the End of each Sampling Scan in Paced operation. It shall be appear “m” times among the Limited operation, where “m” is the number that written to the Paced operation counter specified as section 3-10.

## 3-14. Board Status

```
sts1 = inp (BASE+0xC) ; /* Primary Status */
sts2 = inp (BASE+0xD) ; /* Secondary Status */
```

Read (BASE+CH) and (BASE+DH) Register provides the Status of the Board, and allows the host CPU to watch the operation process in real time.

Table 3-14A. Read (BASE+CH) Register Bit Field

Bit	Term	"=1" specifies	"=0" specifies	On Reset
B7	End of the Paced operation <Note1>	Complete	Not-Complete	0
B6	End of each Sampling scan <Note1>	Complete	Not-Complete	0
B5	Interrupt Over-run Error <Note1>	Occurred	Not-Occurred	0
B4	Over-run Error <Note1>	Occurred	Not-Occurred	0
B3	(FIFO) Data Lost Error <Note1>	Occurred	Not-Occurred	0
B2	(FIFO) Not-Full <Note2>	Not-Full	Full	0
B1	(FIFO) Not-Half-Full <Note2>	Not-Half-Full	Up-Half-Full	0
B0	(FIFO) Not-Empty <Note2>	Not-Empty	Empty	0

## &lt;Note-1&gt;

Bit "B7" "B6" "B5" "B4" "B3" are the latched flags that held the status until reset by the Board Reset, or Write (BASE+CH) Register with the clear command.

## &lt;Note-2&gt;

Bit "B2" "B1" "B0" are the state flags that shall be automatically change with the state of the Paced operation process.

Bit "**B7**" shall be set when the counter decrease to "0" that means the Limited Paced operation is complete.

Note, it must not be set by the Stop Command.

Bit "**B6**" shall be set when the End of each Sampling is complete in Paced operation.

Bit "**B5**" shall be set when the complete-timing of Sampling scan before this time's Sampling scan data are written into the FIFO memory on enabling the interrupt of complete each Sampling scan. Where "Sampling scan" is the element of Paced Update.

Bit "**B4**" shall be set when too much high frequency clock applied as a Pacer Clock.

Bit "**B3**" shall be set when get the fault in Paced Update Operation, because Empty of the FIFO memory.

Bit "**B2**" is the Not-Full state flag that indicates the number of data in the FIFO memory is less than a full state.

Bit "**B1**" is the Not-Half-Full state flag that indicates the number of data in the FIFO memory is less than or equal to a half of its capacity.

Bit "B1=0" means the number of data in FIFO memory is greater than a half of it capacity.

This is very useful for fast block data transfers that should be executed by CPU command with polled status.

Bit "**B0**" is the Not-Empty state flag that indicates the number of data in the FIFO memory is greater than or equal to one. This is very useful for one-by-one data transfers that should be executed by CPU command with polled status.

Table 3-14B. Read (BASE+DH) Register Bit Field

Bit	Term	"=1" specifies	"=0" specifies	On Reset
B7	Not used.			0
B6				0
B5				0
B4				0
B3				0
B2	Interrupt Request <Note1>	Applied	Not-Applied	0
B1	Initial edge of every Pacer Clock <Note1>	Applied	Not-Applied	0
B0	Trigger <Note-3> <Note1>	Applied	Not-Applied	0

## &lt;Note-1&gt;

Bit "B2" "B1" "B0" are the latched flags that held the status until reset by the Board Reset, or Write (BASE+DH) Register with the clear command.

Bit "B2" shall be set when the interrupt request applied.

Bit "B1" shall be set when the valid edge of Pacer Clock applied.

Bit "B0" shall be set when the valid Trigger applied. This Bit shall be reset not only by the Board Reset or Write (BASE+DH) Register with the clear command, but also by Write (BASE+9H) Register as the Trigger source and mode selection.

## &lt;Note-3&gt;

Bit "B0" indicate the state of Digital Trigger Input "TRG-IN" only in case of enabling the External Digital Trigger as a Level.

## Clear Status

```

outp (BASE+0xC, stc1 ) ; /* Clear Status 1 */
outp (BASE+0xD, stc2 ) ; /* Clear Status 2 */

```

Write (BASE+CH) and (BASE+DH) Register work for reset flags individually.

Table 3-14C. Write (BASE+CH) Register Bit Field

Bit	Term	"=1" specifies	"=0" specifies	On Reset
B7	for End of the Paced operation flag	Clear	Non-effect	0
B6	for End of each Sampling scan flag	Clear	Non-effect	0
B5	for Interrupt Over-run Error flag	Clear	Non-effect	0
B4	for Over-run Error flag	Clear	Non-effect	0
B3	for (FIFO) Data Lost Error flag	Clear	Non-effect	0
B2	Not used			0
B1	Not used			0
B0	for all of FIFO memory	Clear	Non-effect	0

Bit "**B0=1**" works to clear the FIFO memory, not only their status but also stored data same as the Board Reset.

Table 3-14D. Write (BASE+DH) Register Bit Field

Bit	Term	"=1" specifies	"=0" specifies	On Reset
B7	Not used.			0
B6				0
B5				0
B4				0
B3				0
B2	for Interrupt Request flag	Clear	Non-effect	0
B1	for Initial edge of every Pacer Clock flag	Clear	Non-effect	0
B0	for Trigger flag	Clear	Non-effect	0

## 3-15. Write Data

**Individual Immediate Direct Output.**

Each Outputs shall be immediately updated individually as a byte data with the write command on Individual Direct Output mode.

**Simultaneous Direct Output.**

Each Output data shall be written into individual waiting register as a byte data, then put Simultaneous output command on Simultaneous Direct Output mode.

## &lt;Procedure&gt;

```

Outp (BASE+0x4, 0x0)  ;/* Set Individual Direct Output mode */
Outp (BASE+0x4, 0x20) ;/* Set Simultaneous Direct Output mode */
Outp (BASE+0x0, P0)   ;/* Write Q00 to Q07 as the port-0 */
Outp (BASE+0x1, P1)   ;/* Write Q08 to Q15 as the port-1 */
Outp (BASE+0x2, P2)   ;/* Write Q16 to Q23 as the port-2 */
Outp (BASE+0x3, P3)   ;/* Write Q24 to Q31 as the port-3 */
Dummy = inp (BASE+0xB) ;/* Simultaneous output command */

```

**Write into FIFO memory for Paced Update.**

Row data is stored temporarily in the FIFO memory until being read out and written into the Output.

It is a byte width register and 2048 byte depth for standard model, also expandable to 16K or 16M byte depth in option.

Each data block consist of one to four byte that specified by Write (BASE+4H) Register as the Output Bit width.

See section 3-7 for details.

## &lt;Procedure&gt; See section 3-2 for the whole process.

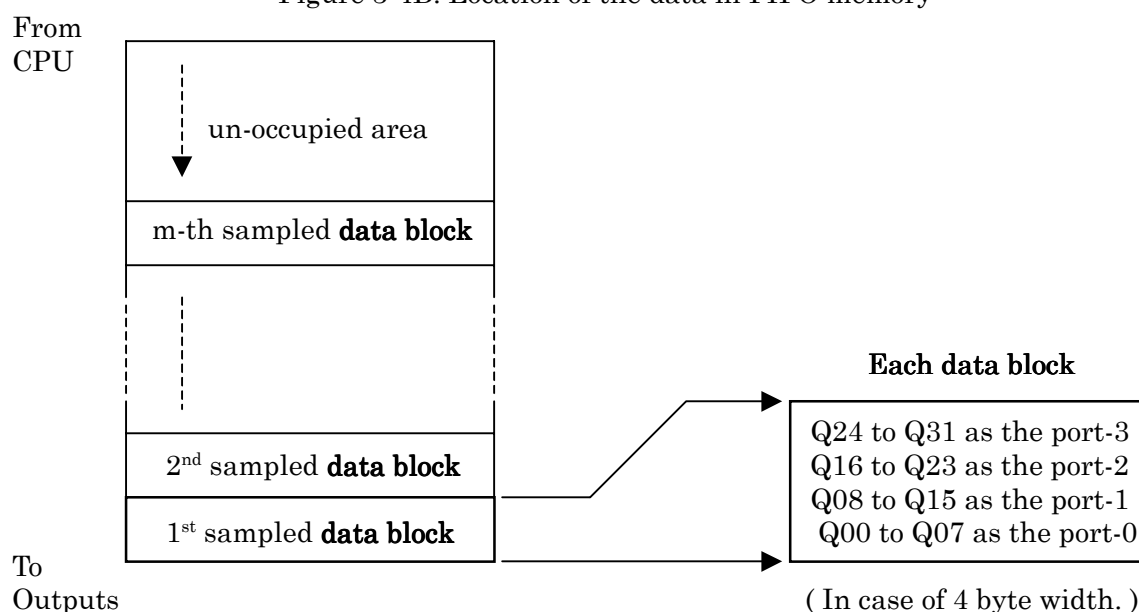
Follows are only one block data write into the FIFO memory for 32-bits width data update.

```

Outp (BASE+0x0, P0) ;/* for Q00 to Q07 as the port-0 */
Outp (BASE+0x0, P1) ;/* for Q08 to Q15 as the port-1 */
Outp (BASE+0x0, P2) ;/* for Q16 to Q23 as the port-2 */
Outp (BASE+0x0, P3) ;/* for Q24 to Q31 as the port-3 */

```

Figure 3-4B. Location of the data in FIFO memory



**<Note for Programming>**

On-board FIFO memory and variety of Status Flags allows the user to program the update or control system in flexible. Follows are typical sample method for writing data by the host CPU.

**Polled status for one-by-one transfer.**

The data may be written by CPU “outp” command when Not-Full state is detected in the software loop.

End of Each Sampling-Scan state is also usable for writing one block data.

**Polled status for block transfer**

The data may be written by CPU “string-outp” command when Half-Full state is detected in the software loop.

**Using Interrupt service.**

The data may be written by CPU “outp” or “string-outp” command in the interrupt service routine triggered by Not-Full, End of Each Sampling-Scan , or Half-Full state.

This method is very useful to execute the seamless data update in back-ground of the application software.

Especially cause Interrupt by Half-Full state and block transfer by CPU “string-outp” command in the interrupt service routine may be usable on the highest update rate of the board so long as the CPU is 386 or better.

### 3-16. Master-Slave Operation

Synchronized Master-Slave operation is also available with multiple boards. Master-board provides the Pacer Clock to the Slave-boards for synchronizing the update between them.

#### On-Board Hardware Configurations.

- (1) Set those Address by the switches SW1, SW2, and SW3 with differences against each other. See section 3-5 for details.
- (2) Set interrupt level by the jumper JP-INT of Master-board if use. See section 3-13 for details.
- (3) Set switch "S-CKZ" to "ON" at only one of the Slave-board, and set to "NC" for the others including Master-board. This is the termination for the Clock Signal.

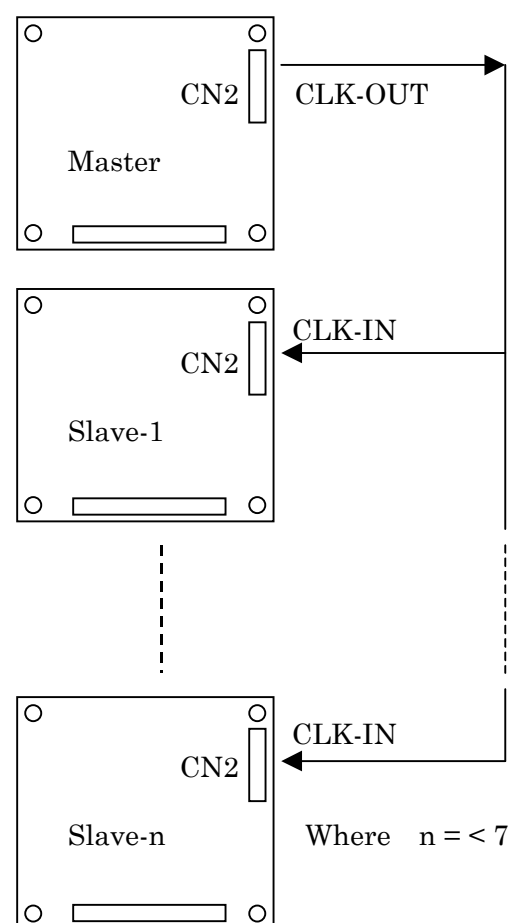
#### Board to Board Connections.

- (1) Pacer Clock Output (CLK-OUT) of Master must be connected to the External Clock Source Input (CLK-IN) of Slaves. Master can drive 7 Slaves directly. If more than 7 Slaves are needed, you can connect the Clock from 7<sup>th</sup> Slave to additional 7 Slaves as well as between Master and Slaves. See figure 3-16.
- (2) External Clock Source Input (CLK-IN) which can be divided and or External Trigger Input (TRG-IN) are available only to the Master.

#### Software Flow.

- (1) Select External Clock Source, and set divide ratio to "1/1" for all slaves. They must accept the Clock Source from the Master.
- (2) Put Software Trigger and Start Command to all Slaves individually as waiting for the Pacer Clock from the Master before enable any Trigger and put Start Command to the Master.
- (3) Paced Operation shall be start by the Trigger to the Master.
- (4) Read data from each FIFO memory by Polled Status or Interrupt Service. See <Note for Programming> in previous section 3-15 for details.

**Figure 3-16.** Master-Slave Connection



## 3-17. General Purpose Digital I/O

Din = inp (BASE+0xE) ; /\* Digital Inputs \*/

outp (BASE+0xE, GPQ) ; /\* General Purpose Digital Output \*/

**Digital Input**

Read (BASE+EH) Register specifies the 3-bits current state external TTL level Inputs “CLK-IN”, “TRG-IN”, and “INT-IN” which assigned on Connector “CN3”.

See Figure 1-7 of section 1-7.

3 External Inputs should work for their own function with the program.

If they have not programmed for the function, they work for General Purpose Digital Input.

Table 3-17A. Read (BASE+EH) Register Bit Field.

Bit	Input assignment	“=1” specifies	“=0” specifies
B7 B6 B5 B4 B3	Not used		
B2	“CLK-IN” as External Clock Source Input	High (or Open)	Low
B1	“TRG-IN” as External Digital Trigger Input	High (or Open)	Low
B0	“INT-IN” as External Interrupt Input	High (or Open)	Low

**Digital Output**

Write (BASE+EH) Register specifies the 1bit of General Purpose Digital Output which

assigned on Connector “CN3”.  
See Figure 1-7 of section 1-7.

Table 3-17B. Write (BASE+EH) Register Bit Field. / **Where S-POL set to “N”** /

Bit	Output assignment	“=1” specifies	“=0” specifies	On Reset
B7 B6 B5 B4 B3 B2 B1	Not used			0 0 0 0 0 0 0
B0	“GPQ-OUT” as General Purpose Digital Output	Low	High	0

## &lt;Note&gt;

Write (BASE+EH) Register is not cleared by Read (BASE+FH) Register as a Board-Reset Command, but cleared by the hardware reset or power-on process.

## &lt;Caution&gt;

Logical Polarity is set to Negative with setting the switch S-POL1 to “N” on shipping cause “GPQ-OUT” to CMOS high state at the hardware reset or power-on process.

Typical 100ms width high state shall be appear on “GPQ-OUT” at the hardware reset or power-on process before set to Low state on Positive Logic with setting the switch S-POL1 to “P”

This is a character of the circuit.



## Section 4. Maintenance and Appendix

### 4-1. Trouble Shootings

#### **Reconfirm.**

The MDI-212PC104 supplied by MICRO SCIENCE is fully inspected and tested. If it doesn't work on your system, reconfirm following issues.

- (1) Check the I/O BASE address specified by the on-board switch SW1, SW2, and SW3. On the IBM PC/AT compatible system, the I/O address must be mapped between "0H" to "3FFH" or the image of this range except for the occupied address by the other devices or the peripherals.
- (2) Debug your software or applications. For example, if the Interrupt level is correct or if occupied by any other devices. Are the Triggers suitable to the application? When the program is waiting for the Triggers, it seems that the program is stacked.
- (3) Be careful to input the signal at the Input of the External Digital Trigger "TRG-IN", Pacer Clock Source "CLK-IN", and Interrupt "INT-IN". Applying the voltage of higher than +7v or lower than -0.5v to these 74HCT-type TTL level inputs shall cause permanent destruction of the front-ended devices. For example, Multi Wave Form Generator is that!

#### **What's wrong?**

Fill in and send (Letter, Fax, or Email) the Q&A form to MICRO SCIENCE where you didn't find anything wrong.

Although we will study about your system and answer by the letter what you should do, we don't write or debug application software.

Sorry, we won't answer with any language but Japanese on the phone. Please write us Japanese or English.

#### **Replace the Board or Repair for free.**

MICRO SCIENCE will replace or repair the Board for free which are after examination disclosed to the satisfaction of MICRO SCIENCE to be thus defective, for a period within one year of shipment. This warranty shall not apply which have been subject to misuse, negligence, or accident. See "Caution/Warranty" for details in page-4.

#### **Repair the Board.**

MICRO SCIENCE will repair, calibrate, or test the Board on request. These products should have to prepaid the transportation at MICRO SCIENCE. Be sure, give us the information with the products, maybe Q&A form is useful for the report.

Then user have to pay the proper cost in few weeks according to the bill after accept the returned products.

## Q & A form (in English or Japanese)

To:  
 MICRO SCIENCE., Co. LTD  
 Customer Support Div  
 2-37-12, Nishiogi-kita,  
 Suginami-ku,  
 Tokyo, Japan

From:

Fax: +81-3-3301-5593  
 Email: [qas@microscience.co.jp](mailto:qas@microscience.co.jp)

Fax:  
 Email:

<b>MDO-212PC104</b>	serial # =	Purchase Date:
Preferences on- Board	SW1 =	JP-INT =
	SW2 =	S-POL =
	SW3 =	S-CKZ=
Other Devices In the system	Product:	
	Occupied Resources: (I/O Address =                      ), (Interrupt =                      )	
System Information	CPU:	
	OS :	
Software	Language:	
	Compiler:	

(Information)

<Note> MICR SCIENCE does not answer on phone with any language but Japanese.