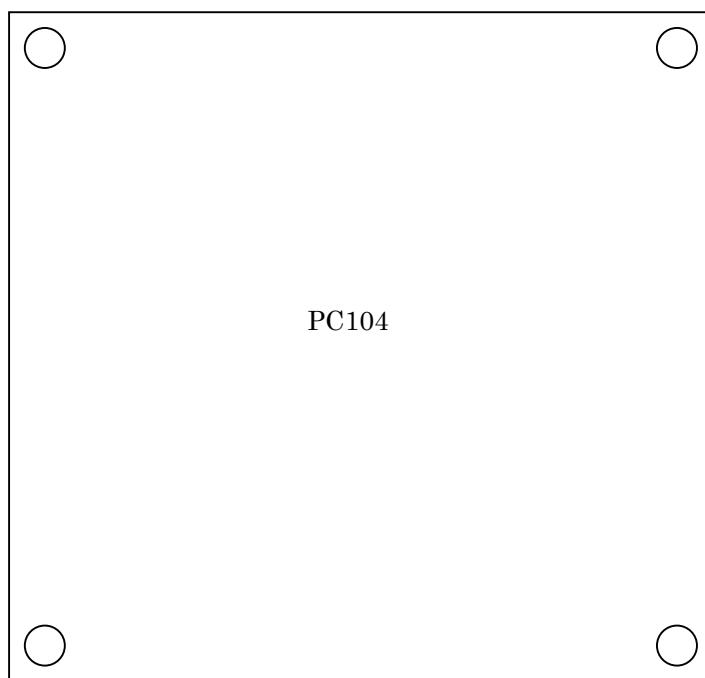


Real Solution for FA & LA



12bit 8ch Single-ended AD Board

ADM-612PC104

User's Manual

For MICRO SCIENCE

PC/104-BUS

AD-Board

MICRO SCIENCE., Co Ltd

2-37-12, Nishiogikita, Suginami-ku,
Tokyo, 167-0042, JAPAN

Phone: +81-3-3396-8362 (Japanese only)

Fax: +81-3-3301-5593 (also English)

Mar 29, 2002

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Caution

Unpacking

This package contain a ADM-612PC104 board, and 4 pieces of 15mm stand-off. Upon receipt the package, visually inspect the board for missing or damaged materials. This product was shipped in perfect condition as it was new. Examine the package for physical damage. In the event of damage, save all packing materials and notify your courier to validate shipping claims.

Anti-static discharge

The ADM-612PC104 contains components that are susceptible to static discharge, and should be handled with appropriate caution. The anti-static packing material protects components from being damaged by static discharge. Should the ADM-612PC104 board need to be returned for repair at a later date, it can be safely done by packing it in the original materials.

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A “PROGRAM” is a file or related group of files which may be loaded and processed on the user’s computer or processing equipment to perform the functions.

A “SOFTWARE” shall mean one or more FILES or PROGRAMS.

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MICRO SCIENCE will answer the written questions including FAX, or Email in Japanese or English from the registered user about this product.
Send us the question form in this manual filled with the information.

We do not answer on phone with any language but Japanese.
Although MICRO SCIENCE may offer advice, we will not design the user's application.

Price List (# on Mar, 2002)

Items	Unit Price	Description
ADM-612PC104	\$ 390.00	12bit / 8 in, 100KHz AD converter board for PC/104
(follows are option)		
User's Manual	\$10.00	Printed one. (PDF file is free for download from WEB)
SHU-008PC104W	\$ 690.00	8in/8out simultaneous sample and hold board

The product consists of a ADM-612PC104 board, 4 pieces of standoff.

WEB : www.microscience.co.jp/eng/

FIFO memory extend Option

A standard ADM-612PC104 board have 1024 word length FIFO buffer memory, at the last stage of the data stream.

We also provide more long FIFO memory on request.

Please add the code next to follow the product name as below.

ADM-612PC104- 8KW : for 8K word length FIFO (Price: add \$100.00)

ADM-612PC104- 1MW : for 1M word length FIFO (Price: add \$220.00)

ADM-612PC104- 8MW : for 8M word length FIFO (Price: add \$340.00)

Section 1. Introduction

1-1. Guide this Manual

This Manual contains a complete set of hardware and programming information for the ADM-612PC104 board, including configuration, installation, and I/O connection.

Section 1 contains the outline of functional descriptions and detail specifications, the installation, and setup procedure for the board.

Section 2 contains the detail of analog input functions, and the digital data.

Section 3 contains the A to D sampling sequence and the post trigger operation.

Section 4 contains the calibration procedure, timing information for the external devices, trouble-shootings, and repair.

The last page is the request form for the Q and A.

1-2. Functional Specification

Analog Input	
####: on-board switch programmable. (typical unless otherwise noted and stated at 20 °C)	
Number of channels	8-SE(single-ended) Inputs
Resolution / Code	12-Bits (4096 counts)
Analog Input Range	-10v to +10v / -5v to +5v / -2.5v to +2.5v ####
Measurement Accuracy	0.105%FS on the range of (-10v to +10v): calibrated 0.125%FS on (-5v to +5v) and (-2.5v to +2.5v).
Non-Linearity	0.025%FS
Input Noise	1LSB (in our test system)
Temperature Coefficient	± 25ppm/°C
Input Impedance	>100M ohm
Input Bias Current	< 50nA
Cross Talk	-65dB (between each channel)

Data Acquisition Mode (selectable in user program)

Acquisition Rate	Up to 100KHz on Paced Acquisition mode.
Paced Acquisition	Input Signals are sampling with the pacer clock synchronously that started by the trigger.
Gated Acquisition	In this mode, It works same as Paced Acquisition, only in the period of software selected External Trigger level.
One-Scan Acquisition	Input Signals are sampling only once with the trigger of software Command.

Control Elements for Data Acquisition**<Note>** TTL level input: 74HCT-type CMOS.

Pacer Clock Source	Internal: 20MHz /accuracy:100ppm/ or External TTL level input (< 10MHz)
Pacer Clock (=Sampling Interval)	Divide the source by 32bit binary counter
Triggers	Software, Analog (compared with Analog Input Channel-0) # Edge, # Level, # Window(Out-Range, In-Range), Levels are 8bit resolution of Analog Input Range. Digital (External TTL level Input): Falling or Rising edge, Level for Gate Acquisition.
Buffer Memory	1K(=1024) words FIFO type, Expandable to 8K, 1M, or 8M words.(see Price List)

General Purpose Digital I/O

Input	3 External Inputs (Clock Source, Digital Trigger, Interrupt) are work for their own function with the program. If they have not programmed for the function, they work for a general purpose (74HCT-type CMOS) TTL level Input.
Output	1 bit (74HCT-type CMOS, latched output)

System Configuration

###: on-board switch programmable.

Bus Compatibility	PC/104 Bus All signals are driven or accepted with the C-MOS device. (74HCT type)
Board Address ###	Higher 12Bits: programmable by on-board switches. Lower 4Bits: on-board logic decoded for multiple I/O ports.
Interrupt ###	IRQ3,4,5,6,7,9

I/O Connectors

Analog Input	34pin FRC type (2.54mm pitch)
Digital Input and Output	10pin FRC type (2.54mm pitch)

Physical, Environmental

Operating Temperature Range	0 to +55
Storage Temperature Range	-10 to +85
Relative Humidity	80% (Non-condensing)
Power Supply, Consumption	+5v 0.5 A

1-3. Functional Description

ADM-612PC104 is designed for multiple analog input channels, can not only get the immediate input levels but also seamless non-stop data acquisition applications. The board accepts analog data up to 8 single-ended inputs.

It is also available master-slave operation for multiple boards by the input and output of the clock.

The analog-to-digital converter has 12 bit resolution, and has a built-in sample-hold element. Analog input range is (-10v to +10v), (-5v to +5v), or (-2.5v to +2.5v), programmable with the on-board Jumper "JP-RNG".

The analog data acquisition rate is up to 100KHz. The paced method allows you to have each sampling-scan process initiated at precise time intervals or synchronized with the external events.

The pacer clock period is software programmable by 32bit binary counter as a divide ratio to the source.

The clock source is also software selectable from internal 20MHz or external TTL level

input.

The software programmed trigger makes the pacer clock start or enable.

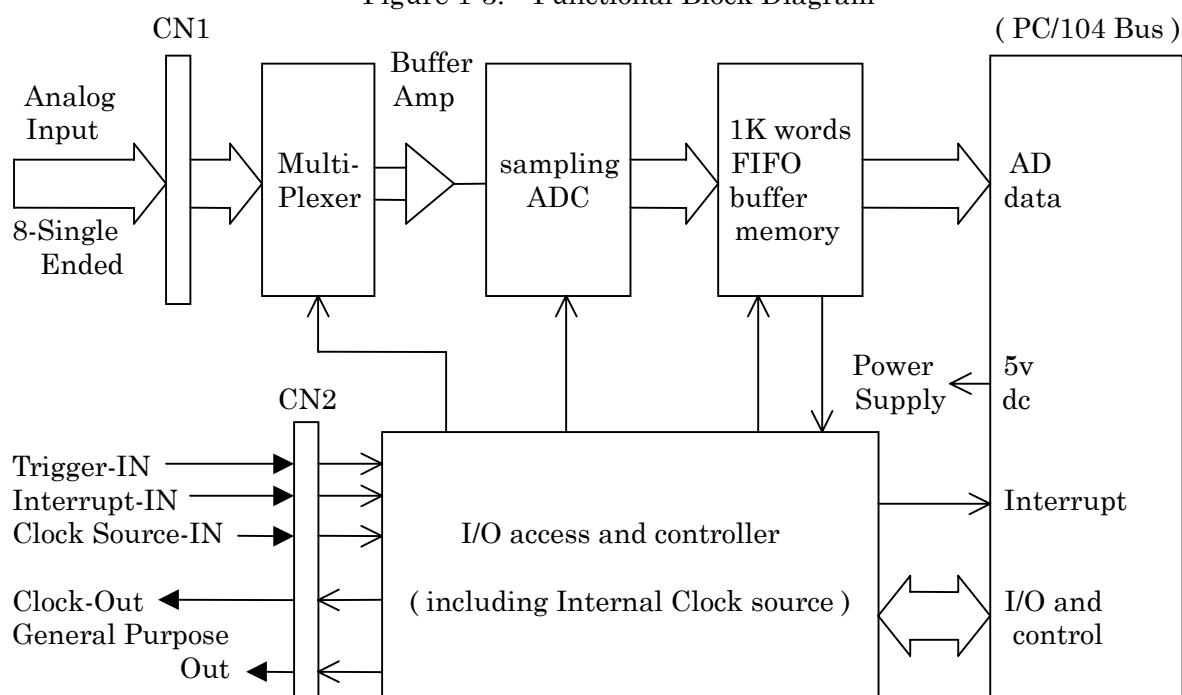
The variety of trigger allows the board to adapted to a wide variety of applications. They are immediate on-software, analog input(Channel-0) edge, level, or External TTL level input edge.

External TTL level Trigger input level can also be used for the gate acquisition.

On-board FIFO type buffer memory allows the user asynchronous AD-data read out from the board. Not-Empty or Half-Full state of the memory can not only usable for read out but also for Interrupt request. Set the jumper-plug on the Interrupt level, if you use the function.

Because against the noise or cross-talk between Analog Input and Digital I/O, they are assigned for individual bracket. The base address of the board is programmable with the on-board switches.

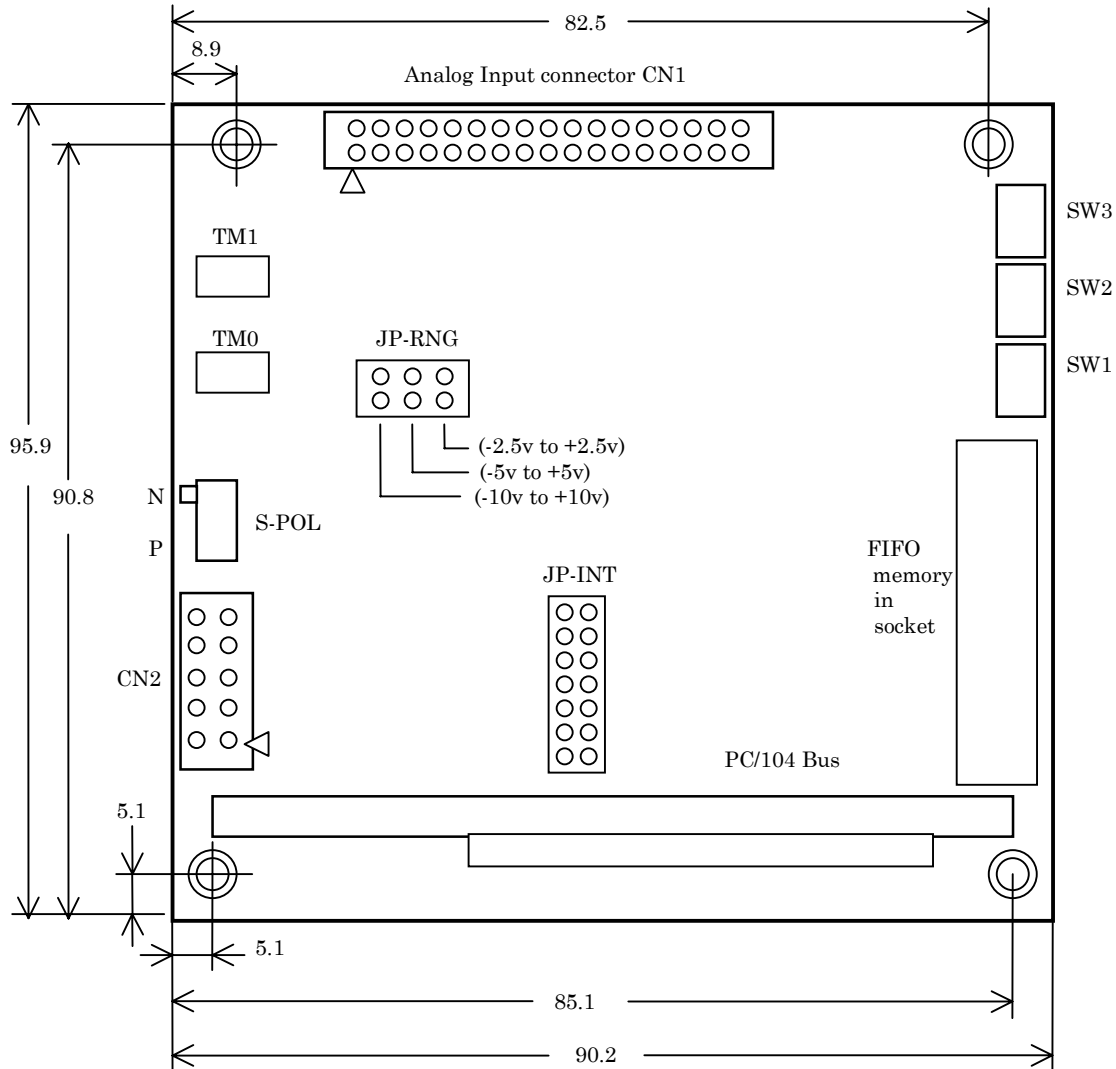
Figure 1-3. Functional Block Diagram



<Note> FIFO memory : Expandable to max.8M words in option.

1-4. Layout of the board

Figure 1-4.



Unit: mm

At shipping, on-board programmable elements are set to < > position.

- # SW1, SW2, SW3: Program switch for Base Address of the board. <0,1,D> / see 1-5-1./
- # JP-INT: Select jumper-switch for Interrupt Level. <NC> ----- / see 1-5-2./
- # S-POL: Select switch for Polarity of General Purpose Output. <N> ----- / see 1-5-3./
- # JP-RNG: Select jumper-switch for Analog Input Range. <-10v to +10v> ---- / see 1-5-4./
- # TM0: POT for offset trimming. ----- / See section 4-2 /
- # TM1: POT for gain trimming. ----
- # CN1: Connector for Analog Input (34pin, FRC) : shows the pin-1
- # CN2: Connector for Digital Input and output (10pin, FRC) : shows the pin-1



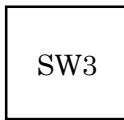
1-5. Settings on the board

1-5-1. BASE ADDRESS

ADM-612PC104 appears as a 16-byte block of registers within the host CPU's I/O address space. This address block must not conflict with other system I/O devices. You can program the on-board switches SW1, SW2, and SW3 as BASE ADDRESS of the board.

These hex-a-decimal defined switches are set to SW1=0, SW2=1, SW3=D at the factory of MICRO SCIENCE, that define the BASE ADDRESS to "01D0" hex. ADM-612PC104 occupies upper 16 byte address from the BASE. See section 3-3 for more information.

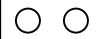
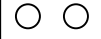
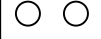
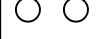



Figure 1-5A. Setting the BASE ADDRESS

Address Line →	AB15 to AB12	AB11 to AB08	AB07 to AB04	AB03 to AB00
On-board Hex-a-decimal → Switches				on-board logic decoded for multiple ports
Factory setting →	0	1	D	(F to 0)

1-5-2. Interrupt Level

Hardware state of ADM-612PC104 can cause an interrupt request to the CPU. Select the interrupt level by the jumper-switch "JP-INT", and program Write (BASE+7H) register to enable the state. See section 3-15 for the details.

Figure 1-5. select the Interrupt Level.

JP-INT	(Level)
	IRQ3
	IRQ4
	IRQ5
	IRQ6
	IRQ7
	IRQ9
	NC (non-connected)

1-5-3. Polarity of Digital Output

ADM-612PC104 has 1 bit CMOS level (74HCT-type) digital output for general purpose. Select the logical polarity of the output by the switch "S-POL".

This switch is set to "N" at the factory of MICRO SCIENCE that defines the logical polarity to "Negative". You can also switch to "P" for "Positive". See section 3-19 for the programming.

1-5-4. Analog Input Mode

Analog Input Range is (-10v to +10v), (-5v to +5v), or (-2.5v to +2.5v), programmable with the on-board Jumper "JP-RNG".

See section 2-1 for more information.

1-6. Analog Input Connector

Analog Inputs are available on a 34-pin FRC-type male connector CN1 on the board as illustrated in Figure 1-4.

8 Single-Ended Analog Inputs are available as CH0 to CH7.

The plug is also provided for general purpose, come with the board.

Figure 1-6. Analog Input Connector CN1 pin assignment

Function	Sign	Pin Assignment			Sign	Function
Digital Common	DG	34	O	O	33	S/H
		32	O	O	31	S/H control output
		30	O	O	29	
		28	O	O	27	
		26	O	O	25	
		24	O	O	23	
		22	O	O	21	
		20	O	O	19	
		18	O	O	17	
Analog Common	AG	16	O	O	15	CH7
Analog Common	AG	14	O	O	13	CH6
Analog Common	AG	12	O	O	11	CH5
Analog Common	AG	10	O	O	9	CH4
Analog Common	AG	8	O	O	7	CH3
Analog Common	AG	6	O	O	5	CH2
Analog Common	AG	4	O	O	3	CH1
Analog Common	AG	2	O	O	1	CH0
					Blank	

<Note.1> AGs are the Analog Common.

They are not only connected each other but also connected with the Digital Common on the board.

<Note.2> S/H is (74HCT-type) CMOS level output that optionally control the External simultaneous sample-hold hardware. See section 2-3 for more information.

<Note.3> On-board bracket : Model=HIF3FC-34PA-2.54DSA /made by HIROSE/
Plug : Model=HIF3BA-34DA-2.54R(11) /made by HIROSE/

1-7. Digital Input and Output Connector

Digital Inputs and Outputs are available on a 10-pin FRC-type male connector CN2 on the board as illustrated in Figure 1-7.

They are External Clock Source Input, External Digital Trigger Input, External Interrupt Input, Pacer Clock Output, and General Purpose latched Output.

All Inputs are (74HCT-type CMOS) TTL level, and pulled-up with 10K resistor.

All outputs are also 74HCT-type CMOS level.

3 External Inputs should work for their own function with the program.

If they have not programmed for the function, they work for General Purpose Digital Input.

See section 3-19 for programming.

The plug is also provided for general purpose, come with the board.

Figure 1-7. Digital Input and Output Connector CN2 pin assignment

Function	Sign	Pin Assignment		Sign	Function
Digital Common	DG	34	O O	33	GPQ-OUT General Purpose Output
Digital Common	DG	32	O O	31	CLK-OUT Clock Output
Digital Common	DG	30	O O	29	CLK-IN External Clock Source Input
Digital Common	DG	28	O O	27	TRG-IN External Trigger Input
Digital Common	DG	2	O O	1	INT-IN External Interrupt Input

<Note.1> DGs are the Digital Common.

They are not only connected each other but also connected with the Analog Common on the board.

<Note.2> On-board bracket : Model= HIF3FC-10PA-2.54DSA /made by HIROSE/

Plug : Model= HIF3BA-10DA-2.54R(11) /made by HIROSE/

1-8. Options (Simultaneous Sampling and Memory)

1-8-1. Simultaneous Sample-Hold module

SHU-008PC104W is 8 channel
Simultaneously Sample and Hold module
for the AD board.

They come with the output cable that is
suitable to adapt the Analog Input of ADM-
612PC104.

Figure 1-8A. Configurations

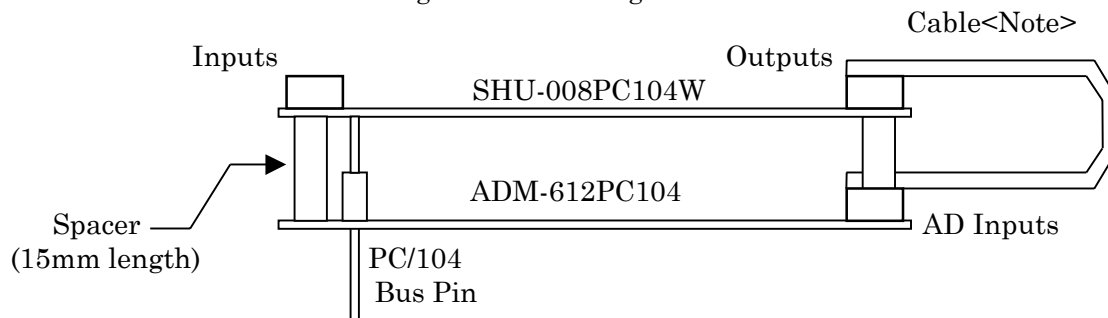
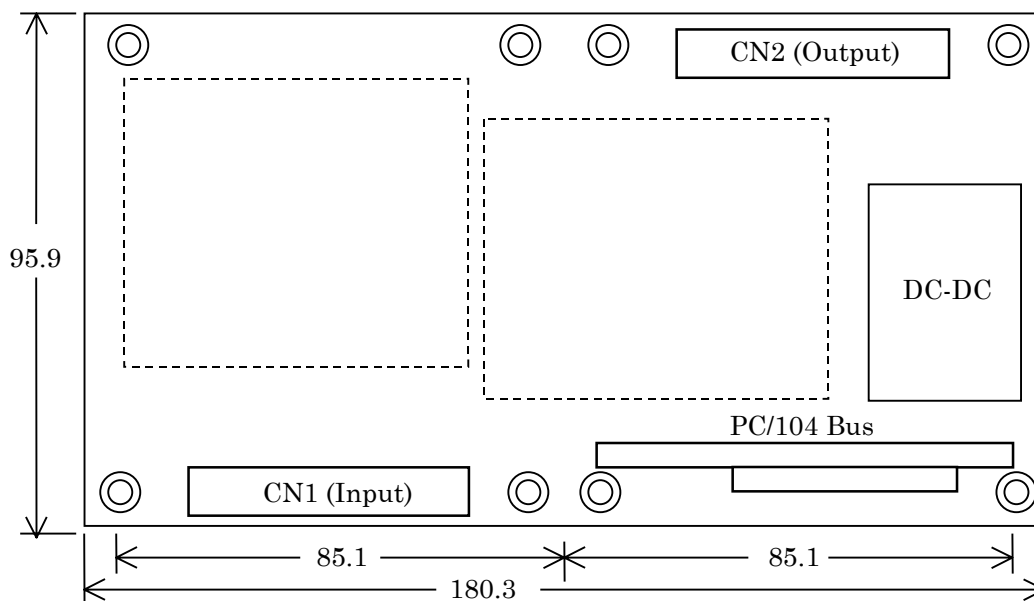


Figure 1-8B. SHU-008PC104W board layout and the Dimensions



1-8-2. FIFO memory Expansion

ADM-612PC104 has 1024 words length
FIFO buffer memory for asynchronous data
read out from the board.
On the typical application, it is enough
capacity to have seamless data-acquisition.

Although on the special application like a
high performance multi-tasking system,
long length FIFO memory may be expected.
MICRO SCIENCE also provide that
expansion to max.8M words length for the
convenience. See Price List for details.

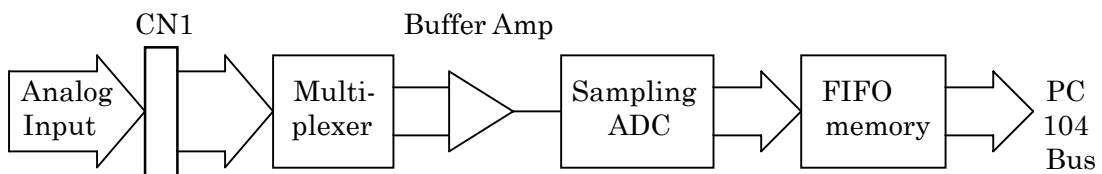
Section 2. Input and Output (details)

2-1. Analog Input

An analog input is selected by the Multi-plexer and input to the A-to-D converter through the Buffer Amplifier, then converted to digital data.

Digital data is automatically written in the FIFO buffer memory, and waiting for read out. These processes are illustrated in Figure 2-1A.

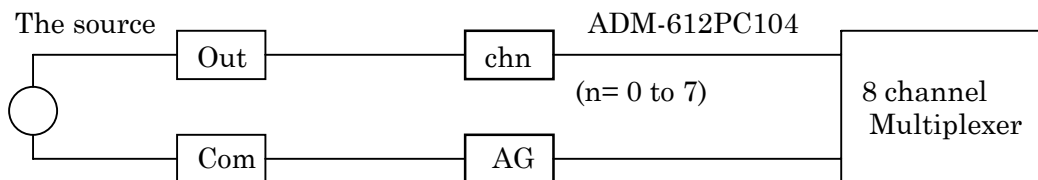
Figure 2-1A. Functional Block



Input Mode.

ADM-612PC104 accepts 8 Single-Ended Analog Inputs.

Figure 2-1B. Analog Inputs (shows only 1 analog input)



2-2. Analog Input Range

The relation between Analog Input and digitized(AD) data for 12-bit offset-binary is follows.

Digitizing Unit,

$$DU = \text{SPAN} \div 4096$$

Where SPAN is the width of the range.

AD data,

$$\text{Dad} = (\text{Vin} \div \text{DU}) + 2048 \text{ digit}$$

Where Vin is Analog Input voltage.

Input voltage,

$$\text{Vin} = (\text{Dad} - 2048) \times \text{DU}$$

Example for -1.5v input
in (-10v to + 10v) range.

$$\begin{aligned} \text{Dad} &= -1.5\text{v} \div (20\text{v} \div 4096) + 2048 \\ &= 1741 \text{ digit} \end{aligned}$$

Example for AD-data = 3000
in (-10v to + 10v) range.

$$\begin{aligned} \text{Vin} &= (3000 - 2048) \times (20 \div 4096) \\ &= 4.648 \text{ v} \end{aligned}$$

Figure 2-2.

Analog Input vs AD data

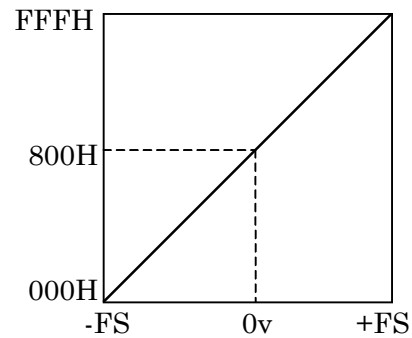


Table 2-2. Analog Input voltage vs AD-data

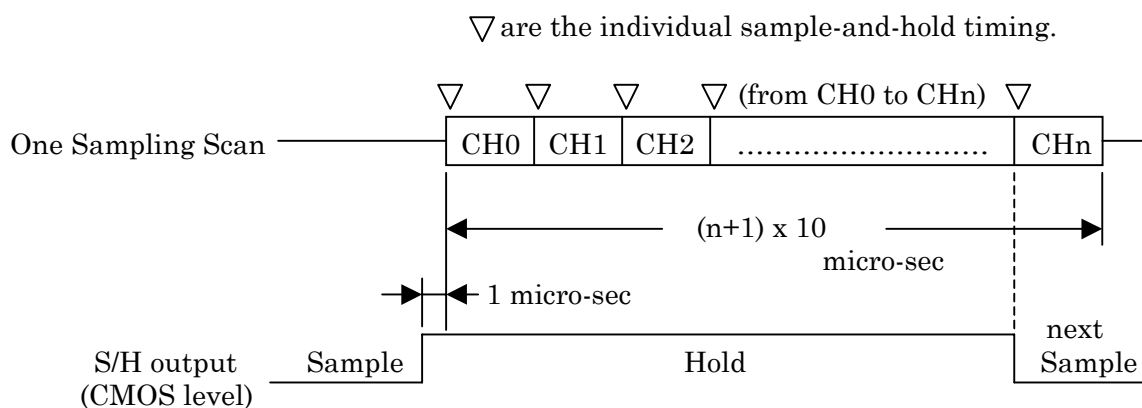
AD-data	Analog Input Voltage <V>			
Hex (Decimal)	-10v to +10v	-5v to +5v	-2.5v to +2.5v	
FFF (4095)	+9.99512	+4.99756	+2.49878	
801 (2049)	+0.00488	+0.00244	+0.00122	
800 (2048)	0.00000	0.00000	0.00000	
7FF(2047)	-0.00488	-0.00244	-0.00122	
001 (0001)	-9.99512	-4.99756	-2.49878	
000 (0000)	-10.00000	-5.00000	-2.50000	

2-3. Simultaneous Sample and Hold

ADM-612PC104 has Sample and Hold function on the front of A-to-D converter. Each Analog Input are sampled and converted sequentially one after another, in case of the board operates on the multi Analog Inputs. Therefore the sampling timing of each Analog Input in the one-scan are not simultaneous.

MICRO SCIENCE also provide 8 Inputs Simultaneous Sample and Hold module.(SHU-008PC104) ADM-612PC104 has "S/H" output assigned on the Analog Input connector CN1 to control the timing of the external Simultaneous Sample and Hold circuits. See section 1-8 for the profile, configuration, and join with ADM-612PC104.

Figure 2-3A. Sequential Sampling scan(on ADM-612PC104) , and External Simultaneous Sample and Hold control output S/H



<Note.1>

ADM-612PC104 operate 10 micro-sec for each Analog Input.

<Note.2>

Write (BASE+FH) Register Command
Optimize the "S/H" Output timing for the Simultaneous Sample and Hold system with the front-ended Multi Sample and Hold circuits. See section 3-20 for details.

2-4. Digital Input and Output

All Digital Inputs are (74HCT-type CMOS) TTL level, and pulled-up to +5v with 10K resistor.

All Digital Outputs are also CMOS level. General Purpose Output is latched output, and you can select the logical polarity by on-board switch S-POL. MICRO SCIENCE set S-POL to “N” as Negative Logic, that cause the output to “CMOS-High” level at power-on reset. General Purpose Output does not clear by the software reset but clear by power-on hardware reset.

Figure 2-4A. Digital Input

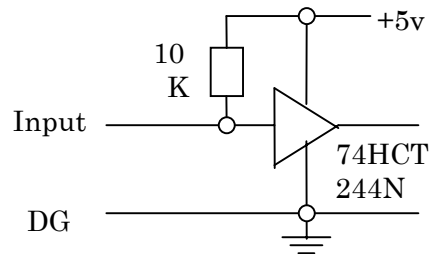
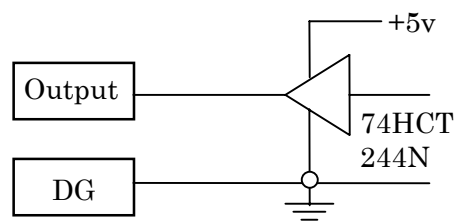


Figure 2-4B. Digital Output



Section 3. General Programming

3-1. General Programming Information

Handling

ADM-612PC104 appears to the host PC/104 bus CPU as a block of contiguous 16 hardware registers mapped within the I/O address space.

These registers control the operation of ADM-612PC104 as long as they are accessed using 16bit I/O addressing with each 8bit data transfers.

These registers include Reset-board, Channels of Sampling object, Pacer Clock, Number of Sampling, Triggers, Start/Stop, Interrupt, Status, AD-data, and General Purpose Digital I/O.

Operation

ADM-612PC104 does the sampling and buffering with on-board FIFO memory, automatically.

It is necessary that the program provides the commands and parameters for the operation.

These are explained in order as follows.
(section 3-2)

General sampling sequences in One-Scan Acquisition Mode and Paced Acquisition Mode.

(section 3-3)

Trigger operations as a start for Paced Acquisition

(section 3-4)

Very useful on-board FIFO buffer memory for seamless sampling.

(section 3-5 to 3-20)

The functions of each register. These are the elements for programming.

3-2. General Sampling Sequence

ADM-612PC104 can operate either One-Scan Acquisition, or Paced Acquisition by the clock.

Both case, each AD-data shall be written into on-board FIFO buffer memory. It is necessary to read out the data from FIFO memory before overflow.

One-Scan Acquisition

This is the operation that execute one sampling for each selected Analog Input. It is only triggered on software for getting the current Analog Input level.

One-Scan Acquisition is executed from Analog Input Channel-0 to selected Channel-n, where “n” is the final channel address of 0 to 7.

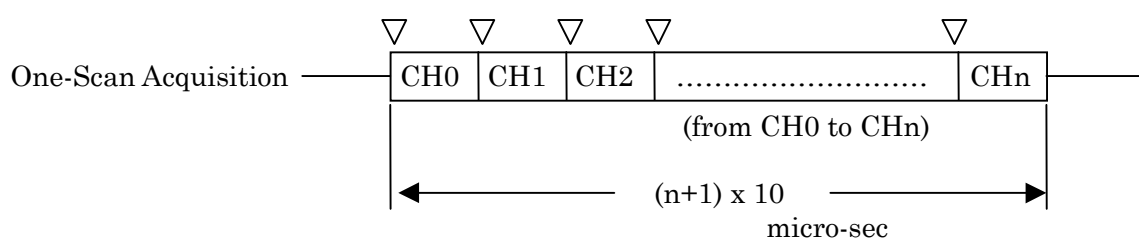
The order of sampling execution is fixed as 0,1,2,3,,,,,N

The sampling execution time for each channel is 10 micro-second, that is also fixed by the hardware logic. They include the time of switching from the previous channel, sample-and-hold, A-to-D conversion, and AD-data writing into the FIFO memory.

----- Procedure of getting AD-data -----

- (1)Reset the board.
<See section 3-6>
- (2)Set Channels.
<See section 3-7>
- (3)Start Acquisition for One-Scan sampling.
<See section 3-14>
- (4)Read Status data and get the timing for read-out the AD-data from FIFO memory.
<See section 3-16>
- (5)Read out the AD-data
<See section 3-17>

Figure 3-2A. Sequential Sampling scan



▽ are the individual sample-and-hold timing.

Paced Acquisition.

The Acquisition is executed continuously at the regular intervals by Pacer Clock.

This method allows you to have each One-Scan Acquisition process initiated at precise time intervals or synchronized with external events

You can specify the Pacer Clock period as an interval time between each One-Scan

Acquisition that is programmable with 32bit binary divide-counter that divide the Clock Source. You can also select the Clock Source from Internal 20MHz or External TTL level input Clock-In.

Whichever clock source you select, you have to program the counter as a divide ratio that makes the Pacer Clock period longer than the One-Scan Acquisition period.

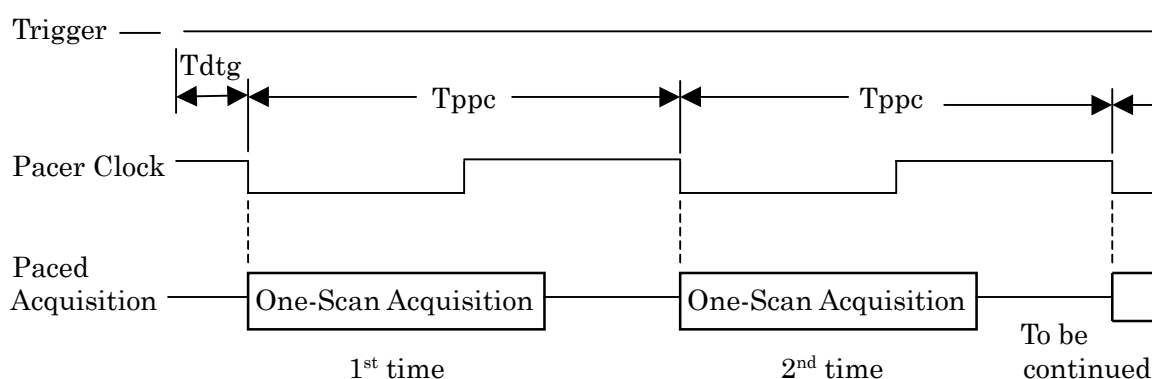
One-Scan Acquisition period is depend on the number of selected channels (n+1) illustrated in Figure 3-2A.

The software programmed trigger including Analog Input Channel-0 state, External Digital Input edge or state, and or the software command makes the Pacer Clock start or enable. Details are explained in the next section 3-3.

----- Procedure of getting AD-data -----

- (1)Reset the board.
<See section 3-6>
- (2)Set Channels.
<See section 3-7>
- (3)Select Pacer Clock Source.
<See section 3-8>
- (4)Set Pacer Clock. (divide ratio)
<See section 3-9>
- (5)Set the Number of Sampling.
<See section 3-10>
- (6)Set Analog Trigger Level. (if use)
<See section 3-11>
- (7)Select the Trigger Source and Mode
<See section 3-12>
- (8)Select the event for Interrupt. (if use)
<See section 3-15>
- (9)Start Acquisition.
<See section 3-13>
- (10)Read Status and get the timing for read out AD-data from FIFO memory.
<See section 3-16>
- (11)Read out AD-data from FIFO memory.
<See section 3-17>

Figure 3-2B. Timing of Paced Method with Internal Clock Source



<Note 1.> Tdtg is the delay after the trigger to initiate the 1st One-Scan Acquisition
 In case of Analog Trigger, Tdtg = 10 micro-second,
 In case of Software command, Tdtg = 125ns.
 In case of External Digital Trigger, Tdtg = 155ns.

<Note 2.> Tppc is the period of Pacer Clock that generated from dividing the Source.

<Note 3.> See section 4-3 for details including Clock output and External Clock Source.

3-3. Variety of Triggers

The software selected trigger makes the Pacer Clock start or enable.

The variety of triggers allow the board to be adapted to a wide range of applications as follows.

See section 3-12 for the programming.

Software Trigger.

You can insert the Software Trigger Command as a immediate start for the Pacer Clock at any time or any point of the application software process.

External Digital Edge Trigger.

When External Digital Edge Trigger is enabled, rising or falling edge of External TTL level input “TRG-IN” makes the Pacer Clock start.

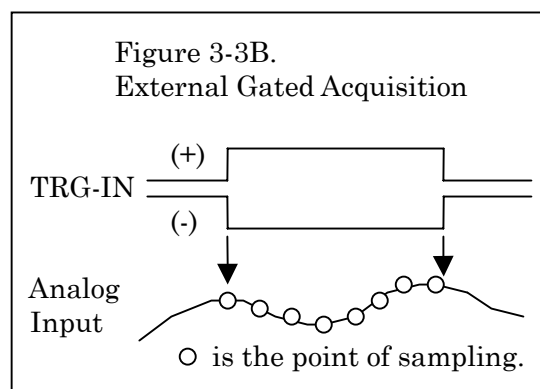
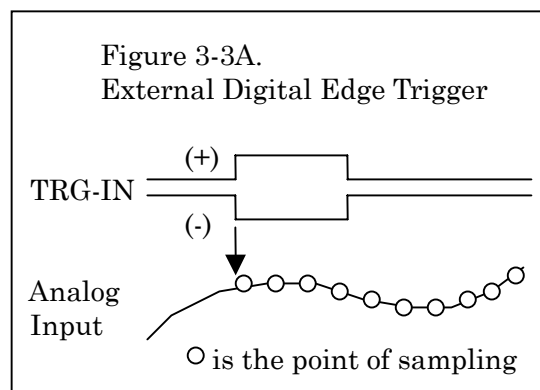
Figure 3-3A shows the operation, in which as a rising edge of “TRG-IN” for trigger is illustrated at upper side, and a falling edge is at lower side. They are also software selectable as a polarity of “+” or “-”.

External Digital Level Trigger.

External TTL level input “TRG-IN” can also be useful for the Gated Acquisition that enable the Pacer Clock as long as the software selectable valid level.

Figure 3-3B shows the work of “TRG-IN” in which “valid level=High” for Gate-On is illustrated at upper side, and “valid level=Low” is at lower side.

Note that another Gate Acquisition shall be executed if another “valid level” come as long as Digital Level Trigger is enabled.



----- Analog Triggers -----

When Analog Trigger is enabled, Analog Input Channel-0 is compared with the software programmed Trigger Level and polarity on the board.

This operation is frequently executed at precise time intervals that is 10 micro-sec until detected the Trigger.

When Analog Trigger is detected, Pacer Clock shall be started or enabled that delayed max 10 micro-sec from the Trigger state.

It is selectable by one of four operation modes, they are Level, Edge, Level-Range, and Edge-Range as follows.

Analog Level Trigger.

In case of the Polarity is programmed to “+”, the Trigger shall be detected when the level of the Analog Input Channel-0 is grater than the programmed Trigger Level. On the other hand, the Polarity is “-”, the Trigger shall be detected when the Input level is less than the Trigger Level.

Analog Edge Trigger.

In case of the Polarity is programmed to “+”, the Trigger shall be detected when the level of Analog Input Channel-0 crosses the programmed two levels in direction from the lower to the grater. On the other hand, the Polarity is “-“, the Trigger shall be detected when the Input Level crosses in the opposite direction.

Analog Range-Level Trigger.

In case of the Polarity is programmed to “+”, the Trigger shall be detected when the level of Analog Input Channel-0 moves to outside of the Range between the programmed two Levels. We call it Out-Range Trigger. On the other hand, the Polarity is “-“, the Trigger shall be detected when the Input level moves to inside of the Range. We call it In-Range Trigger.

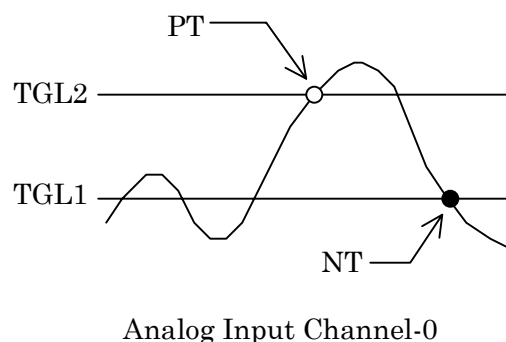
Analog Range-Edge Trigger.

In case of the Polarity is programmed to “+”, the Trigger shall be detected when the level of Analog Input Channel-0 crosses the either side of programmed two levels TGL1 or TGL2 in direction from inside to outside of the Range.

On the other hand, the Polarity is “-“, the Trigger shall be detected when the Input crosses the Level in the opposite direction. <Note>ADM-612PC104 provide the hysteresis levels that are 78mv(=1/256 of the Range) outside from both Levels for against the miss-shot by the noise.

By the way, what is the different between Level Trigger and Edge Trigger?
When ADM-612PC104 starts waiting for the Trigger, Level Trigger can be detected immediately at the Input Level, on the other hand, Edge Trigger can only be detected with the change of the Input Level.

Figure 3-3C. Analog Edge Trigger

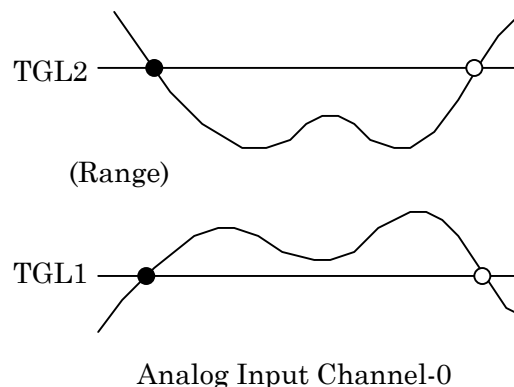


○ :PT is “+” Trigger Timing.

● :NT is “-“ Trigger Timing.

Each Trigger shall be detected at crossing the contiguous two Levels TGL1 and TGL2, where, TGL1 is the Trigger Base Level, TGL2 is the Hysteresis Level, must be $TGL2 > TGL1$, $(TGL2 - TGL1)$ is the Hysteresis against the miss-shot by the noise.

Figure 3-3D. Range-Edge Trigger



○:PT is “+” Trigger Timing.

●:NT is “-“ Trigger Timing.

Each Trigger shall be detected at crossing either two levels TGL1 or TGL2 in each defined direction. where, TGL1 is the High-side Level, TGL2 is the Low-side Level, must be $TGL2 > TGL1$, $(TGL2 - TGL1)$ is the Range.

3-4. On-Board FIFO Memory

On-Board FIFO buffer memory allows the program asynchronous data read out. The Program is always free from taking care of the hardware timing in data read out process while sampling process is being executed on the board.

ADM-612PC104 provides “Not-Empty”, “Not-Half-Full”, and “Data-Lost” flag as the FIFO memory status.

In any time, the program can not only read the Flags for polled method of data read out, but also use them as the trigger for interrupt operation.

Figure 3-4A shows how the FIFO memory works on the board.

The standard model of ADM-612PC104 has 1024 words of data capacity that is enough for many applications.

When the program read the data out from the FIFO memory, un-occupied area shall be expanded up to the capacity. This feature is very useful when the program need to read the data while sampling process is being executed and or need the unlimited acquisition.

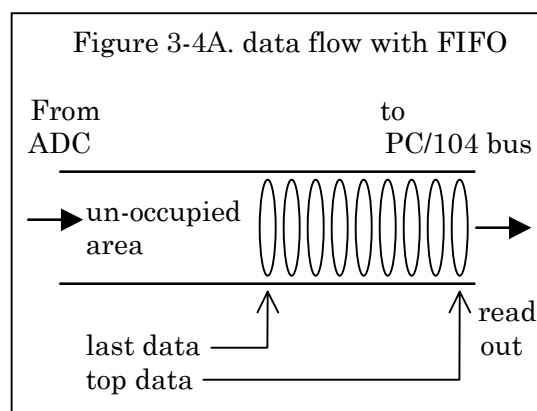


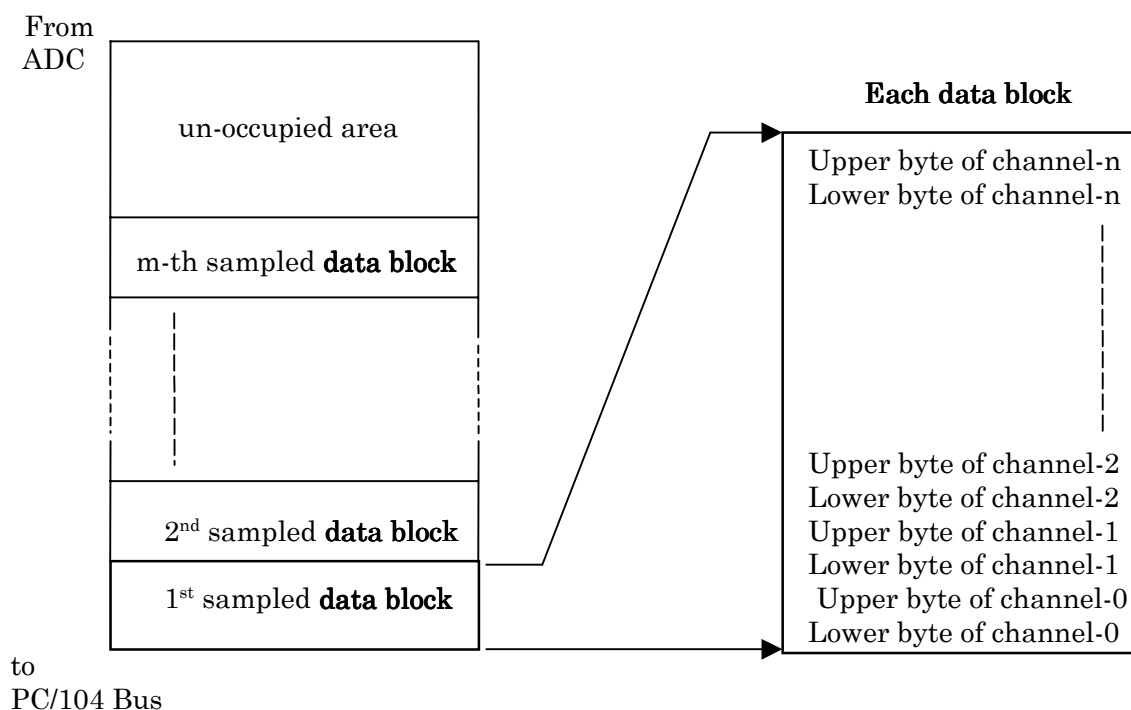
Table 3-4. Status Flag of FIFO memory

item	status
Not-Empty	Occupied one or more.
Not-Half-Full	Not Occupied grater than half of the capacity.
Data Lost	Over flow was happened.

It is possible to expand the capacity of FIFO memory by replace the device.

8K, 1M or 8M words is available at the purchase order in option.

Figure 3-4B. Location of AD-data in FIFO memory



3-5. I/O Register Memory Map

ADM-612PC104 appears as a 16-byte block of registers within the host CPU's I/O address space. This address block must not conflict with other system I/O devices.

You can program the on-board switches SW1, SW2, and SW3 as BASE ADDRESS of the board.

These hex-a-decimal defined switches are set to SW1=0, SW2=1, SW3=D at the factory of MICRO SCIENCE, that specify the BASE ADDRESS to "01D0" hex.

ADM-612PC104 occupies upper 16 byte address from the BASE.

See figure 1-4 for the location of the board.

Figure 1-5A. Setting the BASE ADDRESS




Address Line →	AB15 to AB12	AB11 to AB08	AB07 to AB04	AB03 to AB00
On-board Hex-a-decimal Switches →				on-board logic decoded for multiple ports
Factory setting →	0	1	D	(F to 0)

Table 3-5. ADM-612PC104 Register Assignment. (All the port consist of 8bit.)

I/O Address	Direction	Description	Refer to
BASE +FH	Read	Reset Board, and get ID.	Section 3-6
	Write	Set the Timing for External Sample-Hold	Section 3-20
BASE +EH	Read	External Control Elements Input state.	Section 3-19
	Write	General Purpose Digital Output. (latched)	
BASE +DH	Read	2ndary Status.	Section 3-16
	Write	Clear 2ndary Status.	
BASE +CH	Read	Primary Status.	
	Write	Clear Primary Status.	
BASE +BH	Read		
	Write		
BASE +AH	Read	Start One-Scan Acquisition.	Section 3-14
	Write	Start or Stop for Paced Acquisition.	Section 3-13
BASE +9H	Read		
	Write	Interrupt Source or State.	Section 3-15
BASE +8H	Read		
	Write	Trigger Source and Mode	Section 3-12
BASE +7H	Read		
	Write	Analog Trigger Level-2. (TGL2)	Section 3-11
BASE +6H	Read		
	Write	Analog Trigger Level-1. (TGL1)	Section 3-11
BASE +5H	Read	Acquisition Pacer Clock Counter.	Section 3-10
	Write	Acquisition Pacer Clock Counter.	
BASE +4H	Read		
	Write	Divide Ratio to the Pacer Clock Source.	Section 3-9
BASE +3H	Read		
	Write	Pacer Clock Source.	Section 3-8
BASE +2H	Read		
	Write	Data handling.	Section 3-7
BASE +1H	Read		
	Write		
BASE +0H	Read	AD-data	Section 3-17
	Write	Number of Channels	Section 3-7

3-6. Reset the Board, and get ID

```
rst = inp (BASE+0xF) ; /* Reset the Board */
```

Read (BASE+FH) register cause the board reset.
All registers of the board must be initialized except for the last values of General Purpose Digital Output described in section 3-19.

The acquisition process shall be broken, and previous AD-data in the FIFO memory must be lost.
Where “rst” is the ID that depend on the board, “23H” for ADM-612PC104.

Table 3-6. Read (BASE+FH) Register Bit Field.

Bit	Description
B7	23H is the ID for ADM-612PC104.
B6	
B5	
B4	
B3	
B2	
B1	
B0	

3-7. Analog Input Channel, Data Handling

```
outp (BASE+0x0, n) ; /* final channel address */
```

Write (BASE+0H) Register specifies the channels for acquisition.
From Analog Input Channel-0 to the specified final channel-n shall be sampled on every One-Scan Acquisition that is also executed in the Paced Acquisition.

The order of sampling execution is fixed as 0,1,2,3,,,,,,n.
Table 3-7 shows the structure of the bit field for specifies “n”.
See section 3-2 for more information.

Table 3-7A. Write (BASE+0H) Register Bit Field.

Bit	Term	Parameters	on Reset
B7	Not used		0
B6			0
B5			0
B4			0
B3			0
B2	Final Channel Address of every One-Scan Acquisition.	0H ~ 7H	0
B1			0
B0			0

```
outp (BASE+0x2, hd) ; /* order of reading data, and AD-data code */
```

Write (BASE+2H) Register specifies the data handling and AD-data code.

See section 3-10 and 3-17 for details.

Table 3-7B. Write (BASE+2H) Register Bit Field

Bit	Term	“=0” specifies	“=0” specifies	Reset
B7	Not used.			0
B6	Not used.			0
B5	Not used.			0
B4	Order of reading AD-data and Counter	Upper byte first	Lower byte first	0
B3	Not used.			0
B2	Not used.			0
B1	AD-data code	2’s Compliment	Offset Binary	0
B0	Add digital inputs to AD-data.	Add	Do not add.	0

<Note-B4>

Bit “B4” specifies the order of reading for AD-data and paced acquisition counter.
Where “B4”=0, least significant byte data shall be read first, and most significant byte finally.
Other hand “B4”=1, most significant byte data shall be read first, and least significant byte finally.

<Note-B1>

Bit “B1” specifies the code for AD-data.

<Note-B0>

Set bit “B0”=1 cause assign External Trigger input, Interrupt input, and External Clock Source input into offset-binary coded AD-data bit field.

3-8. Pacer Clock Source Selection

outp (BASE+0x3, cks) ; /* Clock Source */

Write (BASE+3H) register specifies the Pacer Clock Source that should be divided to generate the Pacer Clock.
Table 3-8 shows the structure of the bit field.
The bit “B4” select the Pacer Clock Source either Internal or External of the board.

The bit “B7” select the valid edge of the External Clock Source.
Where, External Clock Source Input “CLK-IN” must be TTL level, and the frequency is less than 10MHz.
Internal Clock Source is 20MHz.

Table 3-8. Write (BASE+3H) Register Bit Field.

Bit	Term	=”1” specifies	=”0” specifies	on Reset
B7	Select the valid edge of “CLK-IN”	Rising edge (+)	falling edge (-)	0
B6	Not used			0
B5				0
B4	Select the Pacer Clock Source	External “CLK-IN”	Internal	0
B3	Not used			0
B2				0
B1				0
B0				0

<Note>

External Clock Source must be less than 10MHz,
and both state of the level must be longer than
45 ns.

3-9. Divide Ratio to Pacer Clock Source

```

outp (BASE+0x4, div0) ; /* 1st data = Least significant byte of divide ratio */
outp (BASE+0x4, div1) ; /* 2nd data = 3rd significant byte of divide ratio */
outp (BASE+0x4, div2) ; /* 3rd data = 2nd significant byte of divide ratio */
outp (BASE+0x4, div3) ; /* 4th data = Most significant byte of divide ratio */

```

Write (BASE+4H) Register specifies the divide ratio to the Pacer Clock Source that specifies the Pacer Clock.
Single 32-bit binary counter must be written 4-byte data in order as describe above.

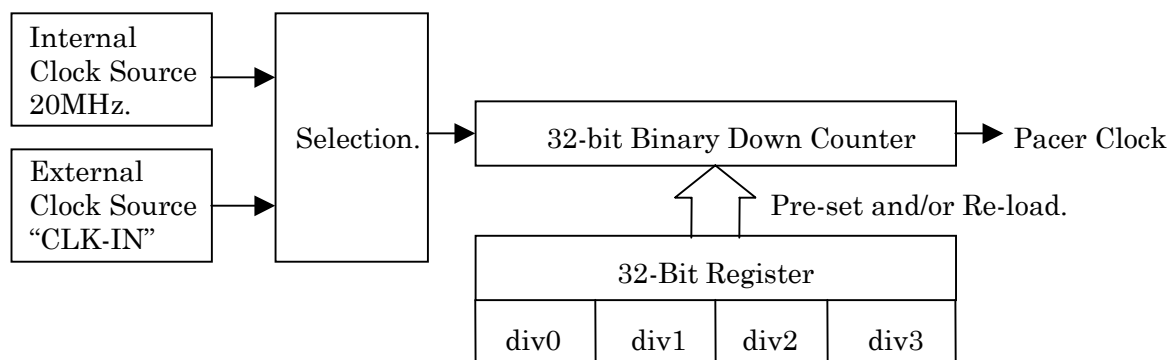
They are held in the same bit-wide registers and automatically re-load the counter at decrease to “0” by down-counting as a divider.

Figure 3-9 shows the configuration of generating Pacer Clock.

Table 3-9. Write (BASE+4H) Register Bit Field.

Bit	1 st data (div0)	2 nd data (div1)	3 rd data (div2)	4 th data (div3)	on Reset
B7	Least significant byte of divide ratio.	3 rd significant byte of divide ratio.	2 nd significant byte of divide ratio.	Most Significant byte of divide ratio.	0
B6					0
B5					0
B4					0
B3					0
B2					0
B1					0
B0					0

Figure 3-9. Configuration of generating Pacer Clock.



3-10. Paced Acquisition Counter

Preset

```

outp (BASE+0x5, num0) ; /* 1st data = Least Significant byte */
outp (BASE+0x5, num1) ; /* 2nd data = 3rd Significant byte */
outp (BASE+0x5, num2) ; /* 3rd data = 2nd Significant byte */
outp (BASE+0x5, num3) ; /* 4th data = Most Significant byte */

```

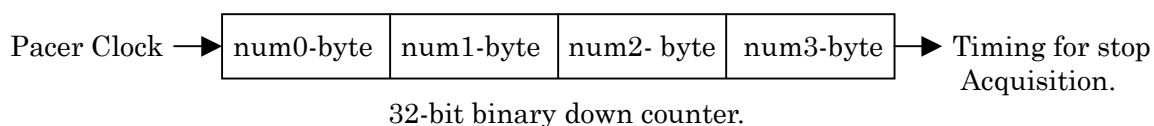
Write (BASE+5H) Register specifies the Number of Acquisition on the Limited Acquisition Mode.
32-bit binary pre-settable down counter must be written as 4-byte data in order as described above.

This Paced Acquisition Counter shall being count down until decrease to “0” on the Limited Acquisition Mode.
Figure 3-10 shows the configuration of Paced Acquisition Counter.
See section 3-13 about the Paced Acquisition Mode.

Table 3-10. Write (BASE+5H) Register Bit Field.

Bit	1 st data (num0)	2 nd data (num1)	3 rd data (num2)	4 th data (num3)	on Reset
B7	Least significant byte.	3 rd significant byte.	2 nd significant byte.	Most Significant byte.	0
B6					0
B5					0
B4					0
B3					0
B2					0
B1					0
B0					0

Figure 3-10. Configuration of Paced Acquisition Counter.



The program can also read out the Paced Acquisition Counter as a rest of the Acquisition times.

This 32-bit binary counter must be read as 4-byte data in order as described below.

Read out

```

Num0 = inp (BASE+0x5) ; /* 1st data = Least Significant byte */
Num1 = inp (BASE+0x5) ; /* 2nd data = 3rd Significant byte */
Num2 = inp (BASE+0x5) ; /* 3rd data = 2nd Significant byte */
Num3 = inp (BASE+0x5) ; /* 4th data = Most Significant byte */

```

<Note>

The order of reading data is change-able to opposite that most significant byte first, least significant byte final.

See section 3-7 for details.

3-11. Analog Trigger Levels

```

outp (BASE+0x6, TGL1) ; /* Trigger Level-1 */
outp (BASE+0x7, TGL2) ; /* Trigger Level-2 */

```

Write (BASE+6H) and (BASE+7H) Register specifies the Levels for Analog Trigger operation.

Specifications of both Levels are defined as Table 3-11C that depend on the Analog Trigger Mode selected with Write (BASE+8H) Register as Table 3-12 described in next section 3-12.

Because both data contains 8-bit wide, they are defined in 1/256 resolution of Analog Input Range.

When ADM-612PC104 is waiting for the trigger, Analog Input Channel-0 is sampled and the higher 8-bit of the Ad-data is compared with the Levels at the interval of 10 micro-second.

See section 3-3 for detail of the Trigger Operation.

Table 3-11A. Write (BASE+6H) Register Bit Field.

Bit	Description	on Reset
B7	1-byte data specifies Analog Trigger Level "TGL1"	0
B6		0
B5		0
B4		0
B3		0
B2		0
B1		0
B0		0

Table 3-11B. Write (BASE+7H) Register Bit Field.

Bit	Description	on Reset
B7	1-byte data specifies Analog Trigger Level "TGL2"	0
B6		0
B5		0
B4		0
B3		0
B2		0
B1		0
B0		0

Table 3-11C. Specification of TGL1 and TGL2

specified parameter	on Edge Trigger Mode	on Level Trigger Mode	on Range Trigger Mode (both Edge or Level)
TGL1	Trigger Base Level	Trigger Base Level	Lower-side Level
TGL2	Hysteresis Level	Dummy data	Higher-side Level

<Note 1> TGL1 or TGL2 is defined as $TGL = V_{tg} / (V_{span} / 256) + 128$ digit
where V_{tg} is the voltage of the level,
 V_{span} is the width of the Analog Input Range.

<Note 2> Dummy data for TGL2 must be written on Level Trigger Mode.

3-12. Trigger Source and Mode

```
outp (BASE+0x8, tgm) ; /* Trigger Source and Mode */
```

Write (BASE+8H) Register specifies the Trigger Mode, Source, and Polarity for the Paced Acquisition.

Bit “B2” and “B3” specifies the Trigger Mode.

Bit “B4” specifies the Polarity of the Trigger Source.

Bit “B5” specifies to enable or disable the Analog Trigger.

Bit “B6” specifies to enable or disable the External Digital Trigger.

Bit “B7” specifies to enable or disable the Software Trigger.

Table 3-12A. Write (BASE+8H) Register Bit Field.

Bit	Term	“=1” specifies	“=0” specifies	on Reset
B7	Software Trigger.	Enable	Disable	0
B6	External Digital Trigger.	Enable	Disable	0
B5	Analog Trigger.	Enable	Disable	0
B4	Polarity of Triggers.	+ (or Rising Edge)	- (or Falling Edge)	0
B3	Trigger Mode.	Edge	Level	0
B2		Range	Except for Range	0
B1	Not used.			0
B0				0

<On and OFF the Paced Acquisition>

Start Command that specified in the next section 3-13 cause ADM-612PC104 into waiting Trigger state, then Paced Acquisition shall be started on detecting any Trigger that enabled, and stopped on the counter decrease to “0” on the Limited Acquisition Mode. Stop Command that specified in the next section 3-13 also cause to stop the Paced Acquisition in any mode.

<Multi Trigger Source>

Because any Trigger Sources are enabled or disabled individually, they work like the switches connected in parallel.

<Delay to Start>

The delay time to start Paced Acquisition with the Internal Clock Source from detect the Trigger is specified as follows.

On Software Trigger; 375ns (max),

On External Digital Trigger ; 405ns (max),

On Analog Trigger ; 10 micro-sec (typ).

Other hand with the External Clock Source, plus 1 Clock Source Period to that value.

<Example>

The procedure of Start Paced Acquisition with the software Trigger is follows.

(1)

Write (BASE+8H) Register to Bit “B7”=1, then Write (BASE+AH) as a Start Command.

or(2)

Write (BASE+AH) as a waiting for Trigger Start Command, then Write (BASE+8H) Register to Bit “B7”=1 as a immediate Trigger.

<Gate Acquisition>

External Digital Level Trigger works as a Gate Acquisition that enabled Write (BASE+8H) Register to Bit “B6”=1, “B3”=0, “B2”=0, and specify the Polarity with “B4”. Paced Acquisition shall be executed among the specified Level.

Table 3-12B. Bit pattern for the Triggers.

Term	B7	B6	B5	B4	B3	B2	State, Source
Software.	1	X	X	X	X	X	Immediate with Command.
Digital (+) Edge.	X	1	X	1	1	0	TTL Rising Edge of "TRG-IN".
Digital (-) Edge.	X	1	X	0	1	0	TTL Falling Edge of "TRG-IN".
Digital (+) Level.	X	1	X	1	0	0	TTL High Level of "TRG-IN".
Digital (-) Level.	X	1	X	0	0	0	TTL Low Level of "TRG-IN".
Analog (+) Edge	X	X	1	1	1	0	Rising Edge of Input Channel-0.
Analog (-) Edge	X	X	1	0	1	0	Falling Edge of Input Channel-0.
Analog (+) Level	X	X	1	1	0	0	Input CH-0 Specified Level.
Analog (-) Level	X	X	1	0	0	0	Input CH-0 Specified Level.
Analog (+) Level Range	X	X	1	1	0	1	Input CH-0 in the Range.
Analog (-) Level Range	X	X	1	0	0	1	Input CH-0 out of the Range.
Analog (+) Edge Range	X	X	1	1	1	1	Input CH-0 go out from the Range.
Analog (-) Edge Range	X	X	1	0	1	1	Input CH-0 go into the Range.

Where "X" is ignored.

----- How the Trigger works for the Paced Acquisition -----

Specified Trigger operate with the Start Command for the post trigger Paced Acquisition as illustrated in Figure 3-12A,B,C.

Although these are illustrated as after Start Command, it is also valid that specify the Trigger before Start Command.

Where ▼ is the start-timing, ▽ is the stop-timing for Paced Acquisition. Paced Acquisition shall be stopped by Stop Command or the counter decrease to “0” on the Limited Acquisition mode.

Figure 3-12A. With the Software Trigger.

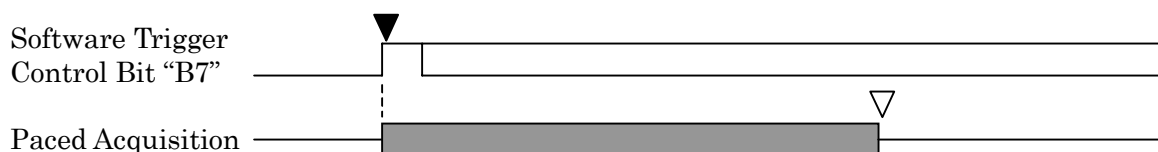
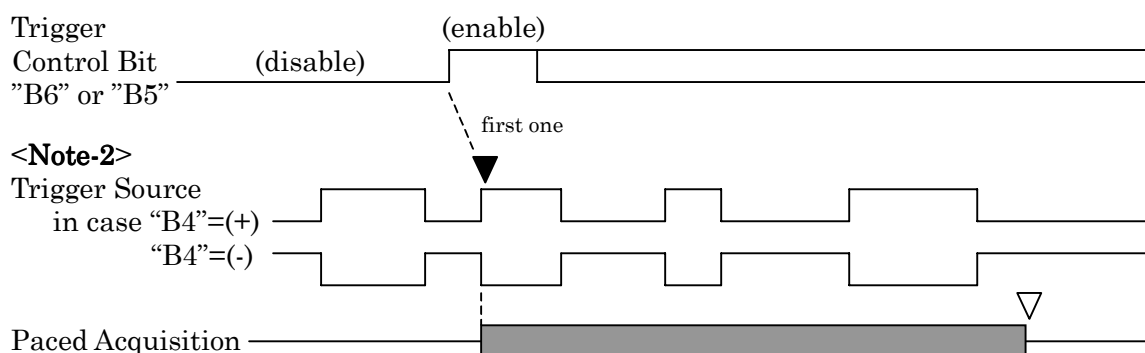


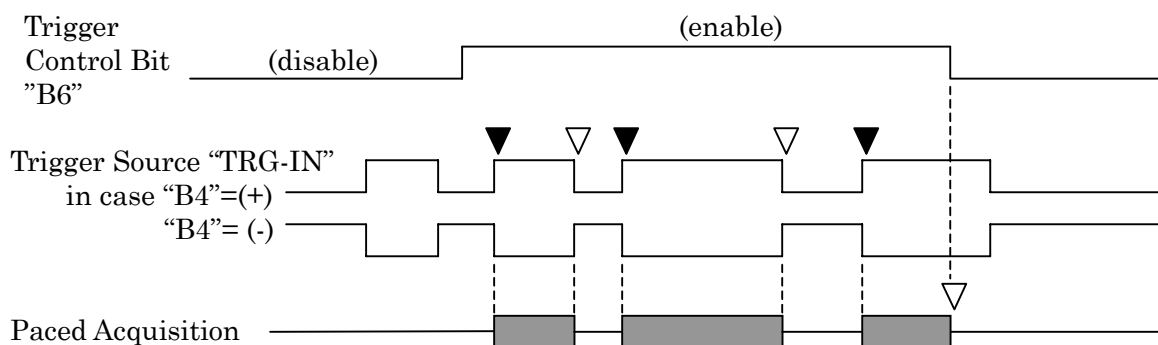
Figure 3-12B. With the (Digital or Analog) Edge Trigger.



<Note-1> After Enable and Start Command, the first valid Edge is the Trigger.

<Note-2> This "Trigger Source" wave form shows in case of Digital Trigger, or against the specified level in case of Analog Trigger.

Figure 3-12C. With the Digital Level Trigger.



<Note> Trigger Mode specify Bits must be set to "B3"=0, "B2"=0.

3-13. Start / Stop Paced Acquisition

out (BASE+0xA, str) ; /* Control the Paced Operation */

Write (BASE+AH) Register specifies the Paced Operation Mode, and ON/OFF control.

Bit “B7” specifies the Paced Operation whether Paced Acquisition or only Pacer Clock run.

Bit “B1” specifies the Paced Operation whether Un-Limited run until “Stop” or Limited run with the Acquisition counter that is specified in section 3-10.

Bit “B0” controls Start and Stop the Paced Operation.

Where “Start” means “waiting for Trigger” that is a post Trigger operation.

ADM-612PC104 is waiting for the Trigger to start the Paced Operation after set “B0”=1, and shall be stopped by set “B0”=0.

Table 3-13A. Write (BASE+AH) Register Bit Field.

Bit	Term	“=1” specifies	“=0” specifies	on Reset
B7	Paced Operation	Pacer Clock only	Paced Acquisition	0
B6	Not used			0
B5				0
B4				0
B3				0
B2				0
B1	Limited / Un-Limited operation.	Limited by counter	Un-Limited	0
B0	Start / Stop Command	Start	Stop	0

Table 3-13B. Bit pattern to control the Paced Operation.

B7	B1	B0	(on post Trigger) Operation
1	1	1	(4) Start Pacer Clock only, Limited run until “counter”=0, or “Stop”.
1	1	0	Stop.
1	0	1	(3) Start Pacer Clock only, un-Limited run until “Stop”.
1	0	0	Stop.
0	1	1	(2) Start Paced Acquisition, Limited run until “counter”=0, or “Stop”.
0	1	0	Stop
0	0	1	(1) Start Paced Acquisition, un-Limited run until “Stop”.
0	0	0	Stop

(1) Un-Limited Acquisition.

This Command cause ADM-612PC104 into waiting for Trigger to start Un-Limited Paced Acquisition that shall run until put “Stop” Command.

(2) Limited Acquisition.

This Command cause ADM-612PC104 into waiting for Trigger to start Limited Paced Acquisition that shall run until count down to “0” of the Acquisition counter or put “Stop” Command.

(3) Un-Limited run only Pacer Clock.

This Command cause ADM-612PC104 into waiting for Trigger to start Un-Limited run only Pacer Clock until put “Stop” Command.

(4) Limited run only Pacer Clock.

This Command cause ADM-612PC104 into waiting for Trigger to start Limited run only Pacer Clock until count down to “0” of the Acquisition counter or put “Stop” Command.

3-14. One-Scan Acquisition

```
dmy = inp (BASE+0xA) ; /* Start One-Scan Acquisition */
```

Read (BASE+AH) Register specifies the Start for One-Scan Acquisition.

Where “dmy” is just a dummy data.

It is available at anywhere on the application software to get the current value of Analog Input Channel-0 to N, where “N” is the final channel address specified by Write (BASE+0H) Register. See section 3-7.

One-Scan Acquisition shall be executed and then transferred into on-board FIFO memory in the period of $\{0.01\text{ms} \times (N+1)\}$, see section 3-2 and 3-4 for details.

<Note>

One-Scan Acquisition is not permitted when Paced Acquisition is running.

----- Sample sequence of Get One-Scan Acquisition data -----

```
RST = inp (BASE+0xF) ; /* Rest the Board */
```

```
Outp (BASE+0x0, N) ; /* Final Channel Address */
```

```
DMY = inp (BASE+0xA) ; /* Start One-Scan Acquisition */
```

```
while ( ( inp(BASE+0xC) & 0x40) != 0x40 ); /* Wait for Ready */
```

```
outp (BASE+0xC, 0x40) ; /* Clear “EOS” of the Status */
```

```
for ( ch=0 ; ch <= N ; ch++ ); /* from Channel-0 to N */
```

```
{
```

```
ADL(ch) = inp (BASE+0x0) ; /* Lower byte of AD-data */
```

```
ADH(ch) = inp (BASE+0x0) ; /* Upper byte of AD-data */
```

```
}
```

3-15. Interrupt Source Selection

```
outp (BASE+0x9, isd ) ; /* Interrupt Source */
```

Write (BASE+9H) Register specifies enable or disable individual Interrupt Source. Hardware state in the ADM-612PC104 that is enabled shall cause an interrupt request to the host CPU.

Interrupt request may be used to synchronize the transfer of AD-data to host CPU or something.

Interrupt Level is specified by the jumper switch “JP-INT” illustrated in Figure 1-5B.

Table 3-15A. Select the Interrupt Level.

“JP-INT”	Level
IRQ 3	3
IRQ 4	4
IRQ 5	5
IRQ 6	6
IRQ 7	7
IRQ 9	9
NC	Non-use

Table 3-15B. Write (BASE+9H) Register Bit Field

Bit	Interrupt Timing	“=0” specifies	“=0” specifies	On Reset
B7	Valid edge of Digital Input “INT-IN”	+ (rising edge)	- (falling edge)	0
B6	“Half-Full” state of FIFO memory	Enable	Disable	0
B5	“Not-Empty” state of FIFO memory	Enable	Disable	0
B4	The End of the Paced Acquisition	Enable	Disable	0
B3	The End of every One-Scan Acquisition	Enable	Disable	0
B2	Detected the Trigger	Enable	Disable	0
B1	Digital Input “INT-IN”	Enable	Disable	0
B0	Initial edge of every Pacer Clock	Enable	Disable	0

Bit “**B7**” specify the valid edge of Digital Input “INT-IN”
If it enabled.

Bit “**B6**” to “**B0**” specify that enable or disable of each
Interrupt Source.

Bit “**B4**” specify that enable or disable to interrupt by
the counter decrease to “0” on Limited Paced Operation.
Note, Stop Command doesn’t work for the Interrupt.

Bit “**B3**” control the interrupt source of the End-Timing of
every One-Scan Sampling of Paced Acquisition.
It shall be appear “m” times among the Limited Acquisition,
where “m” is the number that written to the Paced Acquisition
Counter specified as section 3-10.

<Note>

The New Interrupt Request shall not only be put
but also be set the Over-run Interrupt Error Flag
when the next complete-timing of One-Scan Sampling
before read out previous One-Scan Sampling data
from the FIFO memory.
See next section 3-16 for Over-run Interrupt Error Flag.

3-16. Board Status

```
sts1 = inp (BASE+0xC) ; /* Primary Status */
sts2 = inp (BASE+0xD) ; /* Secondary Status */
```

Read (BASE+CH) and (BASE+DH) Register provides the Status of the Board, and allows the host CPU to watch the acquisition process in real time.

Table 3-16A. Read (BASE+CH) Register Bit Field

Bit	Term	"=1" specifies	"=0" specifies	On Reset
B7	End of the Paced Acquisition <Note1>	Complete	Not-Complete	0
B6	End of One-Scan Acquisition <Note1>	Complete	Not-Complete	0
B5	Over-run Interrupt Error <Note1>	Occurred	Not-Occurred	0
B4	Over-run Error <Note1>	Occurred	Not-Occurred	0
B3	(FIFO) Data Lost Error <Note1>	Occurred	Not-Occurred	0
B2	(FIFO) Not-Full <Note2>	Not-Full	Full	0
B1	(FIFO) Not-Half-Full <Note2>	Not-Half-Full	Up-Half-Full	0
B0	(FIFO) Not-Empty <Note2>	Not-Empty	Empty	0

<Note1>

Bit "B7" "B6" "B5" "B3" are the latched flags that held the status until reset by the Board Reset, or Write (BASE+CH) Register with the clear command.

<Note2>

Bit "B2" "B1" "B0" are the state flags that shall be automatically change with the state of the acquisition process.

Bit "**B7**" shall be set when the acquisition counter go down to "0" that means the Limited Paced Acquisition is complete. Note, it must not be set by the Stop Command.

Bit "**B6**" shall be set when every One-Scan Acquisition in Paced Acquisition is complete.

Bit "**B5**" shall be set when the next complete-timing of One-Scan Acquisition before read out previous One-Scan Acquisition data from the FIFO memory on enabling the interrupt of complete each Sampling scan. Where "One-Scan Acquisition" is the element of Paced Acquisition.

Bit "**B4**" shall be set when too much high frequency clock applied as the Pacer Clock.

Bit "**B3**" shall be set when the new acquisition data is lost at the entrance of the FIFO memory because it full.

Bit "**B2**" is the Not-Full state flag that indicates the number of data in the FIFO memory is less than a full state.

Bit "**B1**" is the Not-Half-Full state flag that indicates the number of data in the FIFO memory is less than or equal to a half of its capacity.

Bit "B1=0" means the number of data in FIFO memory is greater than a half of it capacity. This is very useful for fast block data transfers that should be executed by CPU command with polled status.

Bit "**B0**" is the Not-Empty state flag that indicates the number of data in the FIFO memory is greater than or equal to one. This is very useful for one-by-one data transfers that should be executed by CPU command with polled status.

Table 3-16B. Read (BASE+DH) Register Bit Field

Bit	Term	"=1" specifies	"=0" specifies	On Reset
B7	Not used.			0
B6				0
B5				0
B4				0
B3				0
B2	Interrupt Request <Note1>	Applied	Not-Applied	0
B1	Initial edge of every Pacer Clock <Note1>	Applied	Not-Applied	0
B0	Trigger <Note1>	Applied	Not-Applied	0

<Note1>

Bit "B2" "B1" "B0" are the latched flags that held the status until reset by the Board Reset, or Write (BASE+DH) Register with the clear command.

Bit "**B2**" shall be set when the interrupt request applied.

Bit "**B1**" shall be set when the initial edge of the Pacer Clock applied.

Bit "**B0**" shall be set when the valid Trigger applied. This Bit shall be reset not only by the Board Reset or Write (BASE+DH) Register with the clear command, but also by Write (BASE+8H) Register as the Trigger source and mode selection.

Clear Status

```
outp (BASE+0xC, stc1 ) ; /* Clear Status 1 */
outp (BASE+0xD, stc2 ) ; /* Clear Status 2 */
```

Write (BASE+CH) and (BASE+DH) Register work for reset flags individually.

Table 3-16C. Write (BASE+CH) Register Bit Field

Bit	Term	"=1" specifies	"=0" specifies	On Reset
B7	for End of the Paced Acquisition flag	Clear	Non-effect	0
B6	for End of One-Scan Acquisition flag	Clear	Non-effect	0
B5	for Over-run Interrupt Error flag	Clear	Non-effect	0
B4	for Over-run Error flag	Clear	Non-effect	0
B3	for (FIFO) Data Lost Error flag	Clear	Non-effect	0
B2	Not used			0
B1	Not used			0
B0	for all of FIFO memory	Clear	Non-effect	0

Bit "**B0=1**" works to clear the FIFO memory, not only their status but also stored data same as the Board Reset.

Table 3-16D. Write (BASE+DH) Register Bit Field

Bit	Term	"=1" specifies	"=0" specifies	On Reset
B7	Not used.			0
B6				0
B5				0
B4				0
B3				0
B2	for Interrupt Request flag	Clear	Non-effect	0
B1	for Initial edge of every Pacer Clock flag	Clear	Non-effect	0
B0	for Trigger flag	Clear	Non-effect	0

3-17. Read AD-data

```

ADL= inp (BASE+0x0) ; /* Lower byte of Channel-0 AD-data */
ADH= inp (BASE+0x0) ; /* Upper byte of Channel-0 AD-data */
ADL= inp (BASE+0x0) ; /* Lower byte of Channel-1 AD-data */
ADH= inp (BASE+0x0) ; /* Upper byte of Channel-1 AD-data */
ADL= inp (BASE+0x0) ; /* Lower byte of Channel-2 AD-data */
ADH= inp (BASE+0x0) ; /* Upper byte of Channel-2 AD-data */
.
.
.
ADL= inp (BASE+0x0) ; /* Lower byte of Channel-n AD-data */
ADH= inp (BASE+0x0) ; /* Upper byte of Channel-n AD-data */

```

Read by the host CPU

Row AD-data is stored temporarily in the FIFO memory until being read out by the host CPU. It is a byte-width register. Every AD-data must be read using two sequential access.

The least significant byte is read first, followed by the most significant byte, in order of the Channel Number-0 to n. Where “n” is the final channel address that specified by Write(BASE+0H) Register. See section 3-7 and section 3-4 for details.

Programming Method

On-board FIFO memory and variety of Status Flags allows the user to program the acquisition or control system in flexible. Follows are typical sample method for reading AD-data out by the host CPU.

(1)

Polled status for one-by-one read out.

AD-data may be read by CPU “inp” command when Not-Empty state is detected in the software loop. End of One-Scan Acquisition state is also usable for reading one block data.

(2)

Polled status for block transfer.

AD-data may be read by CPU “string-inp” command when Half-Full state is detected in the software loop.

(3)

Using Interrupt service.

AD-data may be read by CPU “inp” or “string-inp” command in the interrupt service routine triggered by Not-Empty, End of each One-Scan Acquisition, or Half-Full state .

This method is very useful to execute the data acquisition in back-ground of the application software.

Especially cause Interrupt by Half-Full state and block transfer by CPU “string-inp” command in the interrupt service routine may be usable on the highest acquisition rate of the board so long as the CPU is 386 or better.

<Note-1> **AD-data Code.**
AD-data code is specified by Write (BASE+2H) Register, either Offset-Binary or 2’s Compliment. See section 3-7 for details.

<Note-2> **Add digital inputs to AD-data.**
It is available to assign External Trigger input, Interrupt input, and External Clock Source input into offset-binary coded AD-data bit field by Write (BASE+2H) Register. See figure 3-17 and Table 3-17 for details.

<Note-2> **Order of reading AD-data.**
The order of write-in and read-out AD-data for FIFO memory is specified by Write (BASE+2H) Register. Figure 3-4B shows Lower byte first, then Upper byte follows. See section 3-7 for details.

Figure 3-17. Consist of AD-data

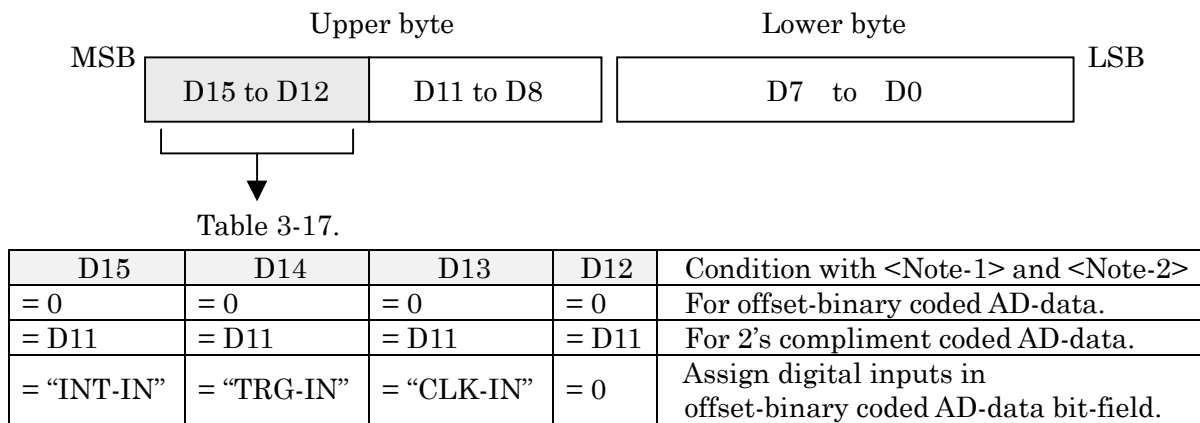
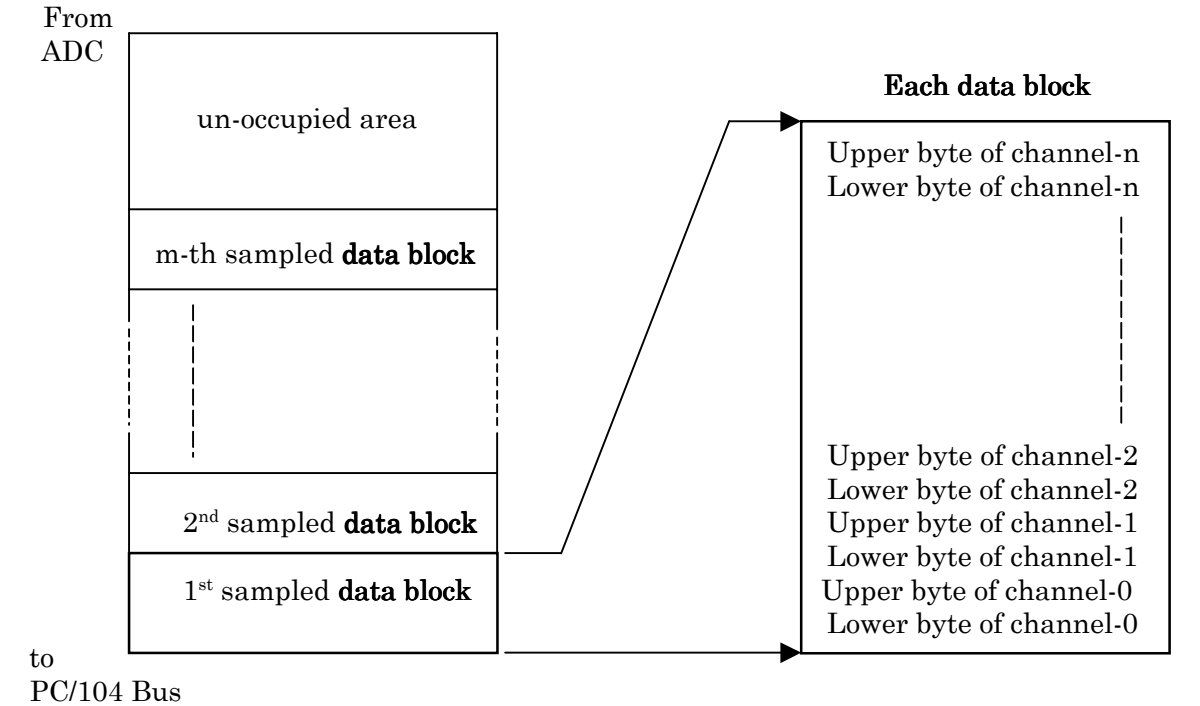


Figure 3-4B. Location of AD-data in FIFO memory



3-18. Master-Slave Operation

Synchronized Master-Slave operation is also available with multiple boards. Master-board provides the Pacer Clock to the Slave-boards for synchronizing the acquisition between them.

On-Board Hardware Configurations.

- (1) Set those Address by the switches SW1, SW2, and SW3 with differences against each other. See section 3-5 for details.
- (2) Analog Input Range is on your choice, any differences between them do not cause trouble.
- (3) Set interrupt level by the jumper JP-INT of Master-board if use.
See section 3-15 for details.

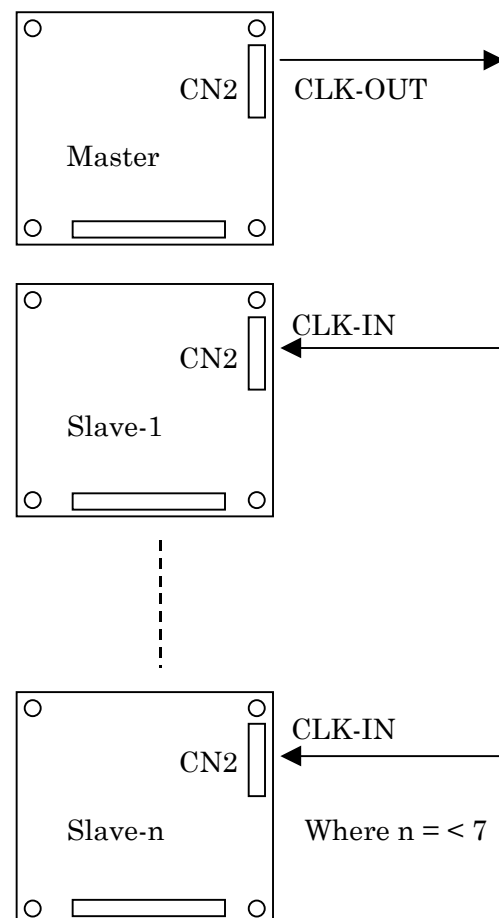
Board to Board Connections.

- (1) Pacer Clock Output (CLK-OUT) of Master must be connected to the External Clock Source Input (CLK-IN) of Slaves. Master can drive 7 Slaves directly. If more than 7 Slaves are needed, you can connect the Clock from 7th Slave to additional 7 Slaves as well as between Master and Slaves. See figure 3-18.
- (2) External Clock Source Input (CLK-IN) which can be divided and or External Trigger Input (TRG-IN) are available only to the Master.

Software Flow.

- (1) Select External Clock Source, and set divide ratio to "1/1" for all slaves. They must accept the Clock Source from the Master.
- (2) Set Software Trigger and Start Command to all Slaves individually as waiting for the Pacer Clock from the Master before enable any Trigger and put Start Command to the Master.
- (3) Paced Acquisition shall be start by the Trigger to the Master.
- (4) Read AD-data from each FIFO memory by Polled Status or Interrupt Service. See <Note for Programming> in previous section 3-17 for details.

Figure 3-18. Master-Slave Connection



3-19. General Purpose Digital I/O

```
Din = inp (BASE+0xE) ; /* Digital Inputs */
outp (BASE+0xE, GPQ) ; /* General Purpose Digital Output */
```

Digital Input

Read (BASE+EH) Register specifies the 3bits external TTL (74HCT-type CMOS) Input “CLK-IN”, “TRG-IN”, and “INT-IN” which assigned on Connector “CN2”.
See Figure 1-7 of section 1-7.

3 External Inputs should work for their own function with the program.

If they have not programmed for the function, they work for General Purpose Digital Input.

Table 3-19A. Read (BASE+EH) Register Bit Field.

Bit	Input assignment	“=1” specifies	“=0” specifies
B7 B6 B5 B4 B3	Not used		
B2	“CLK-IN” as External Clock Source Input	High (or Open)	Low
B1	“TRG-IN” as External Digital Trigger Input	High (or Open)	Low
B0	“INT-IN” as External Interrupt Input	High (or Open)	Low

Digital Output

Write (BASE+EH) Register specifies the 1bit General Purpose (74HCT-type CMOS)

Output which assigned on Connector “CN2”.
See Figure 1-7 of section 1-7.

Table 3-19B. Write (BASE+EH) Register Bit Field. / Where S-POL set to “N” /

Bit	Output assignment	“=1” specifies	“=0” specifies	On Reset
B7 B6 B5 B4 B3 B2 B1	Not used			0 0 0 0 0 0 0
B0	“GPQ-OUT” as General Purpose Digital Output	Low	High	0

<Note>

Write (BASE+EH) Register is not cleared by Read (BASE+FH) Register as a Board-Reset Command, but cleared by the hardware reset or power-on process.

<Caution>

Logical Polarity is set to Negative with setting the switch S-POL to “N” on shipping cause “GPQ-OUT” to CMOS high state at the hardware reset or power-on process. Typical 100ms width high state shall be appear on “GPQ-OUT” at the hardware reset or power-on process before set to Low state on Positive Logic with setting the switch S-POL to “P”
This is a character of the circuit.

3-20. Simultaneous Sample and Hold (Optionally)

outp (BASE+0xF, shc) ; /* Front-ended Sample and Hold control */

Write (BASE+FH) Register specifies the timing of “S/H” Output assigned on Analog Input Connector CN1.

<Normal Mode>

Analog Inputs are selected and converted to Digital Data sequentially from Channel-0 to Channel-N in each One-Scan Acquisition that also consist an element of Paced Acquisition.

In this mode, “S/H” Output is set to CMOS high state among each One-Scan Acquisition process.

<Optimizing Mode>

Select this mode in case of constructing the simultaneous Sample and Hold Acquisition system with the optional Multi Channel Sample and Hold Module like a SHU-008PC104 in front-ended of the Analog Inputs of ADM-612PC104.

In this mode, each One-Scan Acquisition shall be start after 1 micro-sec from the rising (=front) edge of “S/H”.

This timing optimize ADM-612PC104 to the front-ended Multi Channel Sample and Hold Module.

The other hand, that makes 1 micro-sec increase to One-Scan process period cause decrease the maximum sampling frequency as described in Table 3-20B.

Table 3-20A. Write (BASE+FH) Register Bit Field.

Bit	Term	“=1” specifies	“=0” specifies	On Reset
B7	Not used.			0
B6				0
B5				0
B4				0
B3				0
B2				0
B1				0
B0	“S/H” Output Timing	Optimized	Normal	0

Table 3-20B. One-Scan Acquisition **Period** and Maximum Sampling **Frequency**

Mode	Number of Channels >>>	1ch	2ch	4ch	8ch	
Normal	Period (micro-sec)	10	20	40	80	
	Frequency (Hz)	100K	50K	25K	12.5K	
Optimizing	Period (micro-sec)	11	21	41	81	
	Frequency (Hz)	90K	47K	24K	12K	

Section 4. Maintenance and Appendix

4-1. Trouble Shootings

Reconfirm.

The ADM-612PC104 supplied by MICRO SCIENCE is fully calibrated and tested. If it doesn't work on your system, reconfirm following issues.

- (1) Check the I/O BASE address specified by the on-board switch SW1, SW2, and SW3. On the IBM PC/AT compatible system, the I/O address must be mapped between "0H" to "3FFH" or the image of this range except for the occupied address by the other devices or the peripherals.
- (2) Debug your software or applications. For example, if the Interrupt level is correct or if occupied by any other devices. Are the Triggers suitable to the application? When the program is waiting for the Triggers, it seems that the program is stacked.
- (3) Be careful to input the signal at the Input of the External Digital Trigger "TRG-IN", Pacer Clock Source "CLK-IN", and Interrupt "INT-IN". Applying the voltage of higher than +7v or lower than -0.5v to these (74HCT-type CMOS) TTL level inputs shall cause permanent destruction of the front-ended devices. For example, Multi Wave Form Generator is that!

What's wrong?

Fill in and send (Letter, Fax, or Email) the Q&A form to MICRO SCIENCE where you didn't find anything wrong.

Although we will study about your system and answer by the letter what you should do, we don't write or debug application software.

Sorry, we won't answer with any language but Japanese on the phone. Please write us Japanese or English.

Replace the Board or Repair for free.

MICRO SCIENCE will replace or repair the Board for free which are after examination disclosed to the satisfaction of MICRO SCIENCE to be thus defective, for a period within one year of shipment. This warranty shall not apply which have been subject to misuse, negligence, or accident. See "Caution/Warranty" for details in page-4.

Repair the Board.

MICRO SCIENCE will repair, calibrate, or test the Board on request. These products should have to prepaid the transportation at MICRO SCIENCE. Be sure, give us the information with the products, maybe Q&A form is useful for the report.

Then user have to pay the proper cost in few weeks according to the bill after accept the returned products.

4-2. Calibration

ADM-612PC104 is supplied by MICRO SCIENCE fully calibrated and tested . However, before execute the user application and or at the chance of inspection for the system maintenance, you had better to calibrate the Board with the standard source.

Start the program that execute A to D conversion and display the data on screen. Apply reference voltage to the Analog Input of the Board, then trim the potentiometers to have the correct AD-data as shown in Table 4-2.
The adjust points are required only 2 values that represent as the edge of the Range. Take 5 minutes for warm up before calibration to have the specified accuracy.

Procedures.

- (1) Trim the potentiometer "TM0" to have the data "800H" on input voltage is "0v" for the OFFSET adjustment.
- (2) Trim the potentiometer "TM1" to have the data "FFFH" on input voltage is "+10v" for the GAIN adjustment.

Repeat OFFSET and GAIN adjustments alternately until no further accuracy improvement can be obtained.

Table 4-2. Calibration table for ADM-612PC104

Analog Input Range >>>		-10 to +10v	-5 to +5v	-2.5 to +2.5v	0 to 5v	0 to 10v
Offset Trimming	Reference	0v	0v	0v		
	Adjust to	800H	800H	800H		
	Potentiometer	TM0	TM0	TM0		
Gain Trimming	Reference	+9.99512v	+4.99756v	+2.49878v		
	Adjust to	FFFH	FFFH	FFFH		
	Potentiometer	TM1	TM1	TM1		

<Note-1>

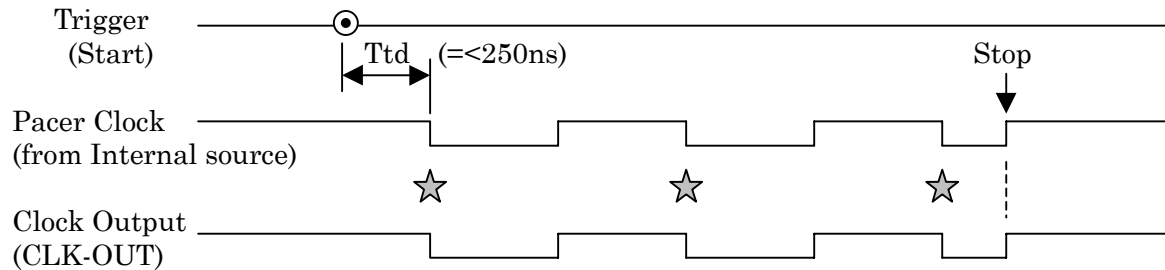
ADM-612PC104 is calibrated within 0.105%FS accuracy for (-10v to +10v) range, and 0.125%FS for the other range, though ADM-612PC104 has 0.025%FS non-linearity.

<Note-2>

The AD-data may be including typical 1-LSB noise in the real application system.

4-3. Trigger and Clock Timing for externals

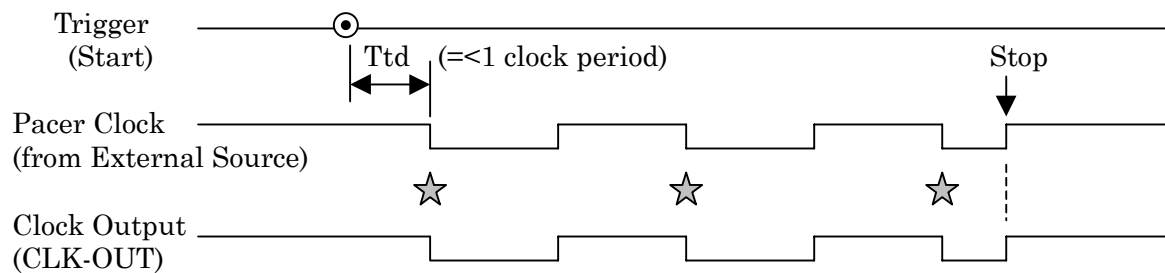
Figure 4-3A. Clock Output with Internal Clock Source



Where T_{td} is the delay from the Trigger to the 1st Pacer Clock.

Valid edge of Pacer Clock and Clock Output is falling. → ☆

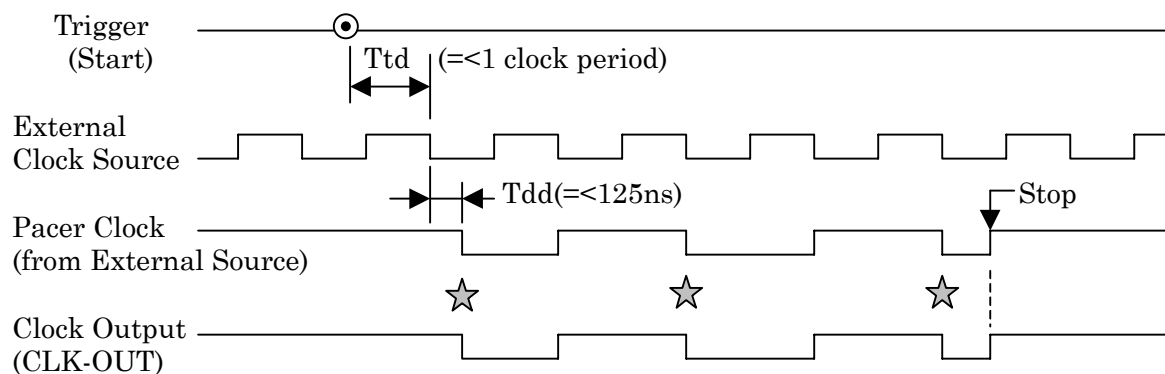
Figure 4-3B. Clock Output with External Clock Source (non-divided)



Where T_{td} is the delay from the Trigger to the 1st Pacer Clock.

Valid edge of Pacer Clock and Clock Output is falling. → ☆

Figure 4-3C. Clock Output with External Clock Source (divided by 2)



Where T_{td} is the delay from the Trigger to the 1st valid External Clock Source.

T_{dd} is the delay of the start to divide for Pacer Clock generation.

Valid edge of Pacer Clock and Clock Output is falling. → ☆

Q & A form (in English or Japanese)

To:
MICRO SCIENCE., Co. LTD
Customer Support Div
2-37-12, Nishiogi-kita,
Suginami-ku,
Tokyo, Japan

From:

Fax: +81-3-3301-5593
Email: gas@microscience.co.jp

Fax:
Email:

ADM-612PC104	serial # =	Purchase Date:
Preferences on- Board	SW1 =	JP-RNG =
	SW2 =	S-POL =
	SW3 =	JP-INT =
Other Devices In the system	Product:	
	Occupied Resources: (I/O Address =), (Interrupt =)	
System Information	CPU:	
	OS :	
Software	Language:	
	Compiler:	

(Information)

<Note> MICR SCIENCE does not answer on phone with any language but Japanese.