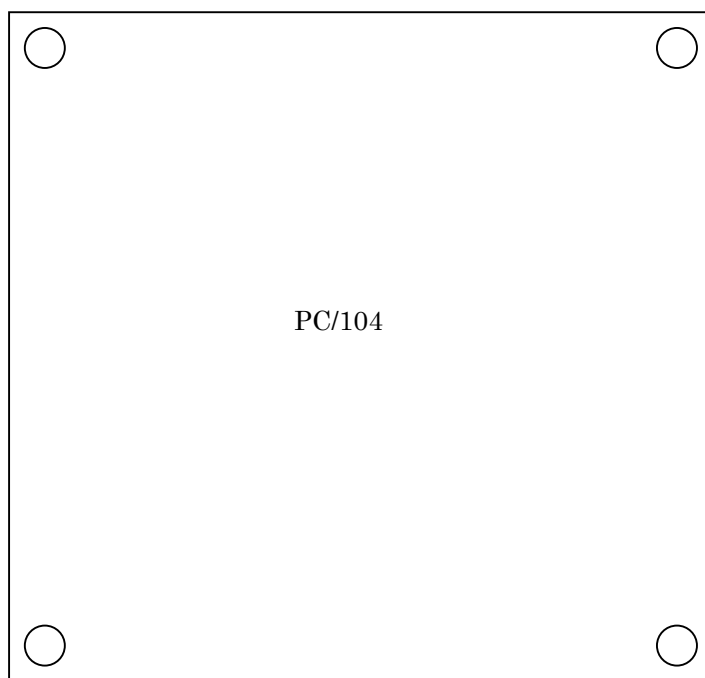


## Real Solution for FA & LA



12bit 4ch Analog Output with FIFO memory

# MDA-714PC104

## User's Manual

For MICRO SCIENCE

PC/104-BUS

DA-Board

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## Table of Contents

Caution .....	4
Legal Notice .....	4
Software License Agreement .....	5
Customer Support .....	6
Price List and Ordering Information .....	6

## Section 1. Introduction

1-1. Guide this Manual .....	7
1-2. Functional Specification .....	7
1-3. Functional Description .....	9
1-4. Layout of the Board .....	10
1-5. Settings on the Board .....	11
1-6. Analog Output Connector .....	12
1-7. Digital Input and Output Connector .....	13

## Section 2. Input and Output (details)

2-1. Analog Output configuration .....	15
2-2. Analog Output Range .....	16
2-3. Digital Input and Output .....	17

## Section 3. General Programming

3- 1. General Programming information .....	19
3- 2. General Sampling Sequence .....	20
3- 3. Variety of Triggers .....	25
3- 4. On-Board FIFO memory .....	26
3- 5. I/O Register Memory Map .....	27
3- 6. Reset the Board, and get ID .....	28
3- 7. Analog Output Mode, Channel, Range .....	29
3- 8. Pacer Clock Source Selection .....	31
3- 9. Divide Ratio to the Pacer Clock Source .....	32
3-10. Paced Operation Counter .....	33
3-11. Trigger Source and Mode .....	35
3-12. Start/Stop Paced Operation .....	37
3-13. Interrupt Source Selection .....	39
3-14. Board Status .....	40
3-15. Write DA-data .....	43
3-16. Master Slave Operation .....	45
3-17. General Purpose Digital I/O .....	46

## Section 4. Maintenance and Appendix

4-1. Trouble Shootings .....	47
4-2. Calibration .....	48
4-3. Trigger and Clock Timing for Externals .....	49
4-4. Q & A form .....	50

## Caution

### Unpacking

This package contain a MDA-714PC104 board and 4 pieces of 15mm stand-off.

Upon receipt the package, visually inspect the board for missing or damaged materials. This product was shipped in perfect condition as it was new.

Examine the package for physical damage. In the event of damage, save all packing materials and notify your courier to validate shipping claims.

### Anti-static discharge

The MDA-714PC104 contains components that are susceptible to static discharge, and should be handled with appropriate caution. The anti-static packing material protects components from being damaged by static discharge.

Should the MDA-714PC104 board need to be returned for repair at a later date, it can be safely done by packing it in the original materials.

### Warranty

MICRO SCIENCE warrants that this product was manufactured free of defect in materials or workmanship under normal use and service as described in this User's Manual. Obligations under this warranty are limited to replacing or repairing at MICRO SCIENCE's option.

Any said of products, at MICRO SCIENCE's factory or facility, should have to be prepaid transportation charges, and which are after examination disclosed to the satisfaction of MICRO SCIENCE to be thus defective, for a period within one year shipment.

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The information contained in this document has been carefully examined and is believed to be entirely accurate.

However, MICRO SCIENCE assumes no responsibility for errors or omissions.

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In this Agreement, a “FILE” shall mean a contiguous collection of machine-readable symbols, bytes, characters, or codes which may be used by the CPU on the user’s computer or processing equipment.

A “PROGRAM” is a file or related group of files which may be loaded and processed on the user’s computer or processing equipment to perform the functions.

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## Customer Product Support Policy

MICRO SCIENCE will answer the written questions(including FAX,Email) in Japanese or English from the registered user about this product.

Send us the question form in this manual filled with the information.

We do not answer on phone with any language but Japanese.

Although MICRO SCIENCE may offer advice, we will not design the user's application.

### Price List (# on Feb, 2002)

Items	Unit Price	Description
MDA-714PC104	\$ 440.00	12-bit / 4 out DA converter board for PC/104
User's Manual	\$10.00	Printed one. (PDF file is free for download from WEB)

# The product consists of a MDA-714PC104 board and 4 pieces of standoff.

**WEB :** [www.microscience.co.jp/eng/](http://www.microscience.co.jp/eng/)

### **FIFO memory extend Option**

A standard MDA-714PC104 board have 1024 word length FIFO buffer memory, at the first stage of the data stream.

We also provide more long FIFO memory on request.

Please add the code next to follow the product name as below.

**MDA-714PC104- 8KW :** for 8K word length FIFO (Price: add \$100.00)

**MDA-714PC104- 1MW :** for 1M word length FIFO (Price: add \$220.00)

**MDA-714PC104- 8MW :** for 8M word length FIFO (Price: add \$340.00)

## Section 1. Introduction

### 1-1. Guide this Manual

This Manual contains a complete set of hardware and programming information for the MDA-714PC104 board, including configuration, installation, and I/O connection.

**Section 1** contains the outline of functional descriptions, detail specifications, installation, and setup procedure for the board.

**Section 2** contains the detail of analog output functions, and the digital data.

**Section 3** contains the D to A sampling sequence and Paced Operation.

**Section 4** contains the calibration procedure, timing information for the external devices, trouble-shootings, and repair.

The last page is the request form for the Q and A.

### 1-2. Functional Specification

<b>Analog Output</b>	(typical unless otherwise noted and stated at 20 °C)
Number of channels	4 Outputs
Resolution / Code	12Bits (4096 counts) / Binary
Analog Output Range (software selectable)	-10v to +10v / -5v to +5v / 0 to +5v / 0 to +10v
Accuracy	0.07 %FS
Non-Linearity	0.004%FS
Glitch	400 mv
Temperature Coefficient	25ppm/°C
Settling time	8 micro-sec (10v swing to 0.1%FS on 100pF load )
Slew rate	5v/micro-sec
Output Impedance	< 0.5 ohm
Driving Capability	5K ohm, 500pF
0v Output on Reset	Return to 0v on Reset Command or Power-on process.

#### **Analog Output Mode** (selectable with user program)

Sampling Rate	Up to 2MHz on Paced Update mode.
Paced Update	Analog Outputs are sampling in accordance with the pacer clock that start with the trigger.
Gated Update	In this mode, It works same as Paced Update, only within the period of software selected External Digital Trigger level.
Manual Update	Analog Outputs are updated only once by the software Command.

**Control Elements for Paced Operation.**


---

Pacer Clock Source	Internal: 20MHz /accuracy :100ppm /, or External 74HCT-type CMOS input (< 10MHz)
Pacer Clock (=Sampling Interval)	Divide the source by 32bit binary counter
Triggers	Software, Digital (External 74HCT-type CMOS Input) Falling or Rising edge, Level for Gated Output.
Buffer Memory	1K(=1024) words FIFO type, Expandable to 8K, 1M, or 8M words.(see Price List)

**General Purpose Digital I/O**


---

Input	3 External Inputs (Clock Source, Digital Trigger, Interrupt) are work for their own function with the program. If they have not programmed for the function, they work for a general purpose 74HCT-type CMOS Input.
Output	1 bit (74HCT-type CMOS level, latched output)

**System Configuration**


---

Bus Compatibility	PC/104 Bus All signals are driven or accepted with the C-MOS device. (74HCT type)
Board Address	Upper 12Bits: programmable by on-board switches. Lower 4Bits: on-board logic decoded for multiple I/O ports.
Interrupt	(selectable on-board switches if use)

**I/O Connectors**


---

Analog Output	16pin FRC type (2.54mm pitch)
Digital Input and Output	10pin FRC type (2.54mm pitch)

**Physical, Environmental**


---

Operating Temperature Range	0 to +55
Storage Temperature Range	-10 to +85
Relative Humidity	80% (Non-condensing)
Power Supply, Consumption	+5v 0.6 A



### 1-3. Functional Description

MDA-714PC104 is designed for multiple analog output channels, can not only update immediately but also seamless non-stop data output applications.

The board provides analog data up to 4 single-ended outputs.

It is also available master-slave operation for multiple boards by the input and output of the clock.

The digital-to-analog converter has 12 bit resolution, and output range is software-selectable from 0 to +10v, 0 to +5v, -5 to +5v, and -10 to +10v that specifies individually for each output.

The analog data output rate is up to 2MHz. The paced method allows you to have each update-scan process initiated at precise time intervals or synchronized with the external events.

The pacer clock period is software programmable by 32-bit binary counter as a divide ratio to the source.

The clock source is also software selectable from internal 20MHz or external input. The software programmed trigger makes the pacer clock start or enable.

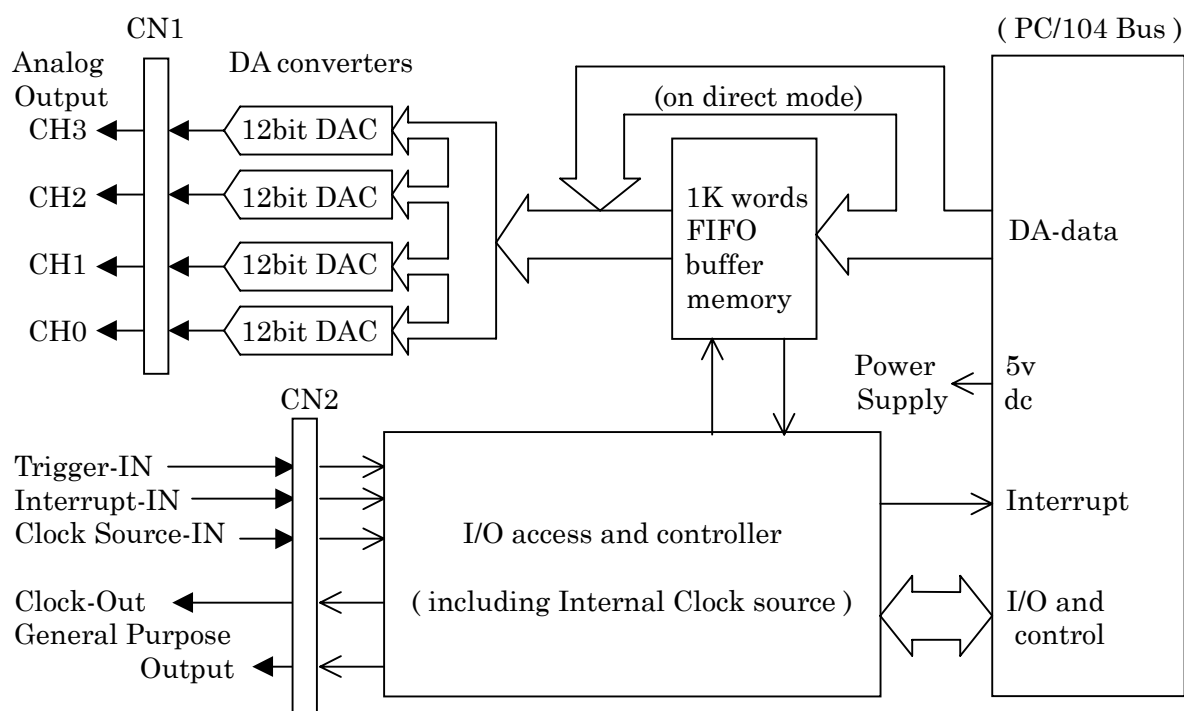
The variety of trigger allows the board to be adapted to a wide variety of applications. They are immediate on-software, External input edge, or level.

External Trigger input level can also be used for the gated output.

On-board FIFO type buffer memory allows the user asynchronous DA-data write into the board. Not-Full or Half-Full state of the memory is not only usable for polled method but also for Interrupt request. Set the jumper-plug on the Interrupt level, if you use the function.

Because against the noise or cross-talk between Analog Output and Digital I/O, they are assigned for individual bracket. The base address of the board is programmable with the on-board switches.

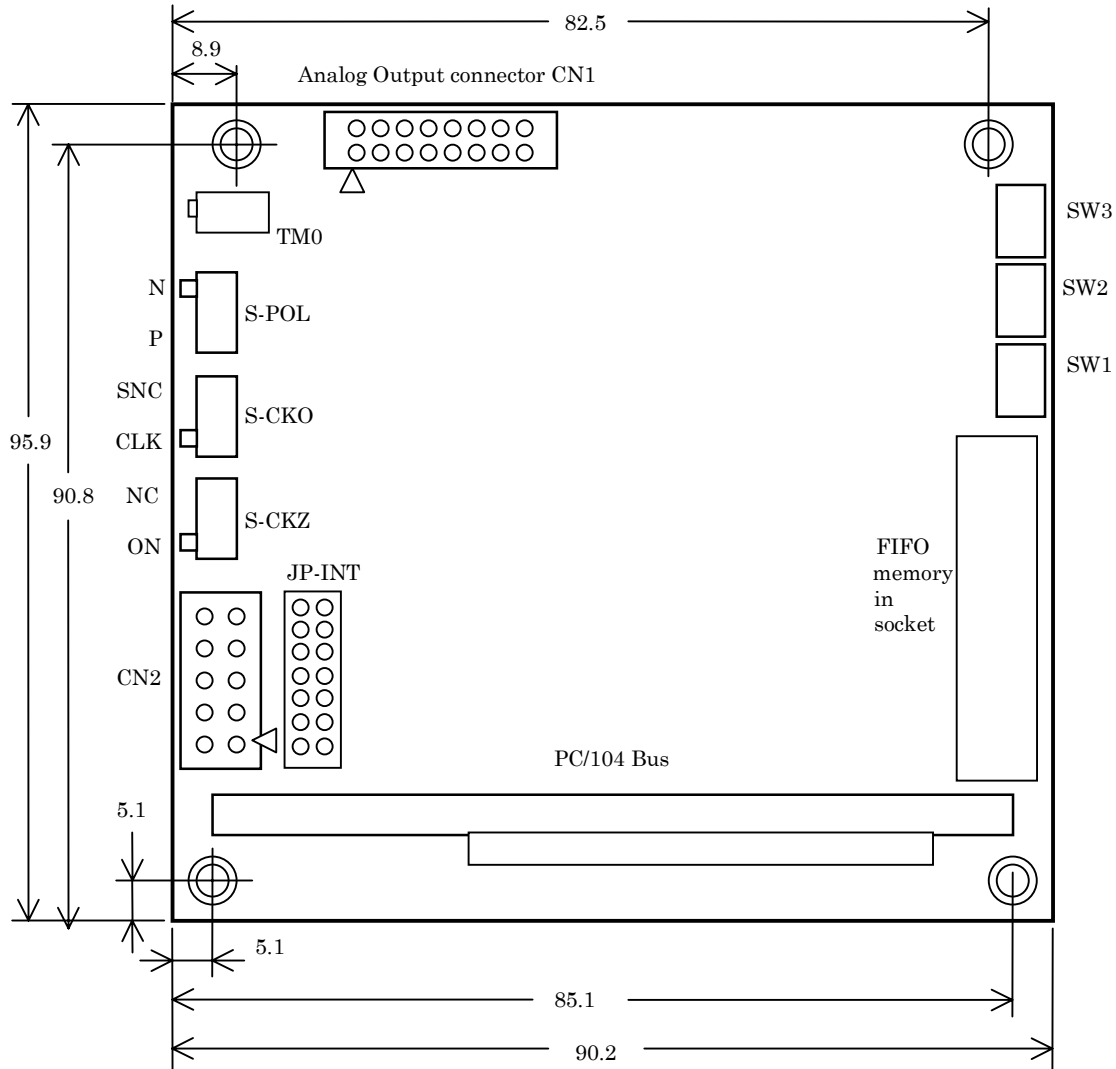
Figure 1-3. Functional Block Diagram



<Note> FIFO memory is Expandable to max.8M words in option.

## 1-4. Layout of the board

Figure 1-4.



Unit: mm

At shipping, on-board programmable elements are set to < > position.

- # SW1, SW2, SW3: Program switch for Base Address of the board. <0,1,E> / see 1-5-1./
- # JP-INT: Select jumper-switch for Interrupt Level. <NC> / see 1-5-2./
- # S-POL: Select switch for Polarity of General Purpose Output. <N> / see 1-5-3./
- # S-CKO: Select switch for Control Output. <CLK> / see 1-5-4./
- # S-CKZ: Select switch for Clock Signal Terminator connection. <ON> / see 1-5-4./

# TM0: POT for gain trimming

# CN1: Connector for Analog Output (16pin, FRC) : shows the pin-1

# CN2: Connector for Digital Input and output (10pin, FRC) : shows the pin-1

## 1-5. Settings on the board

### 1-5-1. BASE ADDRESS

MDA-714PC104 appears as a 16-byte block of registers within the host CPU's I/O address space. This address block must not conflict with other system I/O devices.



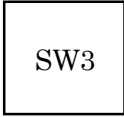
You can program the on-board switches SW1, SW2, and SW3 as BASE ADDRESS of the board.

These hex-a-decimal defined switches are set to SW1=0, SW2=1, SW3=E at the factory of MICRO SCIENCE, that define the BASE ADDRESS to "01E0" hex.

MDA-714PC104 occupies upper 16 byte address from the BASE.

See section 3-3 for more information.

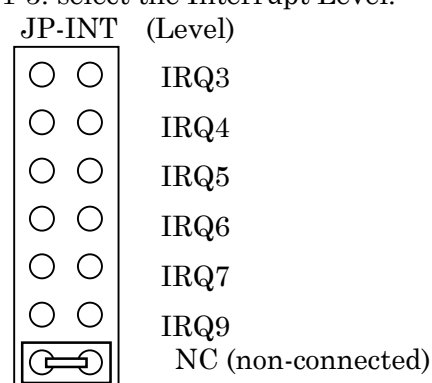
Figure 1-5A. Setting the BASE ADDRESS

Address Line →	AB15 to AB12	AB11 to AB08	AB07 to AB04	AB03 to AB00
On-board Hex-a-decimal → Switches				on-board logic decoded for multiple ports
Factory setting →	0	1	E	( F to 0 )

### 1-5-2. Interrupt Level

Hardware state of MDA-714PC104 can cause an interrupt request to the CPU. Select the interrupt level by the jumper-switch "JP-INT", and program Write (BASE+9H) register to enable the state. See section 3-15 for the details.

Figure 1-5. select the Interrupt Level.



### 1-5-3. Polarity of Digital Output

MDA-714PC104 has 1 bit HCT-type CMOS level digital output for general purpose. Select the logical polarity of the output by the switch "S-POL".

This switch is set to "N" at the factory of MICRO SCIENCE that defines the logical polarity to "Negative".

You can also switch to "P" for "Positive". See section 3-19 for the programming.

### 1-5-4. Timing Control Output and Clock Input Termination.

MDA-714PC104 provides the Timing Control Output "CLK-Out" for the external devices. It is selectable either "CLK" for Pacer Clock Output or "SNC" for Top of the cycle Timing Output in Cycle Output Mode by on-board switch "S-CLK".

In case of using the External Clock Source, "CLK-IN" must be terminated with the resistors by set the on-board switch "S-CKZ" to "ON". In case of Master-Slave operation, set switch "S-CKZ" to "ON" at only one of the Slave board and set to "NC" for the others including Master board.

See section 3-16 for more information.

## 1-6. Analog Output Connector

Analog Outputs are available on a 16-pin FRC-type male connector CN1 on the board as illustrated in Figure 1-4.

The plug is also provided for general purpose, come with the board.

Figure 1-6. Analog Output Connector CN1 pin assignment

sign	/ Function /	pin assign		sign / Function /
CH0	Analog Output ch0	1	2	AG /analog common/
CH1	Analog Output ch1	3	4	AG /analog common/
CH2	Analog Output ch2	5	6	AG /analog common/
CH3	Analog Output ch3	7	8	AG /analog common/
		9	10	
		11	12	
		13	14	
		15	16	

<Note.1> AGs are Analog Common.

They are not only connected each other but also connected with Digital Common on the board.

<Note.2> On-board bracket : Model=HIF3FC-16PA-2.54DSA /made by HIROSE/  
 Plug : Model=HIF3BA-16DA-2.54R(11) /made by HIROSE/

## 1-7. Digital Input and Output Connector

Digital Inputs and Outputs are available on a 10-pin FRC-type male connector CN2 on the board as illustrated in Figure 1-7.

They are External Clock Source Input, External Digital Trigger Input, External Interrupt Input, Pacer Clock Output, and General Purpose latched Output.

All Inputs are TTL input level, and pulled-up with 10K ohm resistor.

All outputs are 74HCT-type CMOS level.

3 External Inputs should work for their own function with the program.

If they have not programmed for the function, they work for General Purpose Digital Input.

See section 3-17 for programming.

The plug is also provided for general purpose, come with the board.

Figure 1-7. Digital Input and Output Connector CN2 pin assignment

sign	/Function/	pin assign	sign /Function/
INT-IN	External Interrupt Input	1	DG /Digital common/
TRG-IN	External Digital Trigger Input	3	DG /Digital common/
CLK-IN	External Clock Source Input	5	DG /Digital common/
CLK-OUT	Pacer Clock Output <Note 2>	7	DG /Digital common/
GPQ-OUT	General Purpose Digital Output	9	DG /Digital common/

<Note.1> DGs are the Digital Common.

They are not only connected each other but also connected with Analog Common on the board.

<Note.2> “CLK-OUT” is selectable either “**CLK**” for Pacer Clock Output or “**SNC**” for Top of the cycle Timing Output in Cycle Output Mode by on-board switch “S-CLK”.

<Note.3> On-board bracket : Model = HIF3FC-10PA-2.54DSA /made by HIROSE/  
Plug : Model = HIF3BA-10DA-2.54R(11) /made by HIROSE/



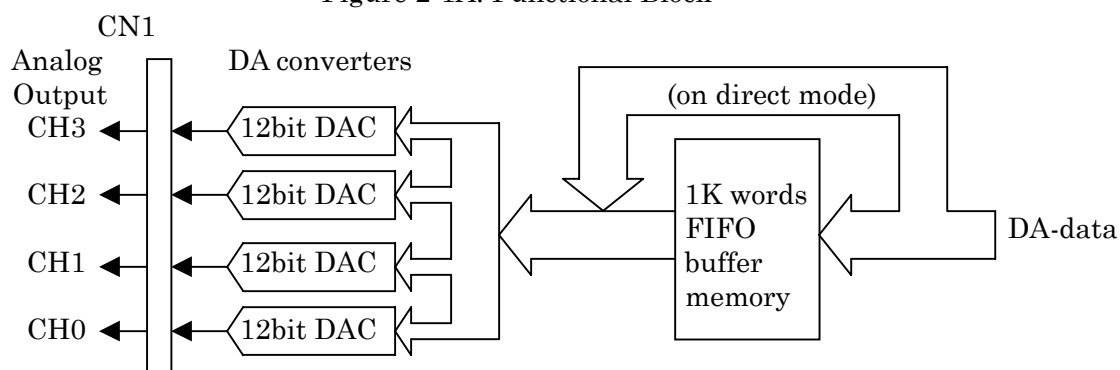
## Section 2. Input and Output (details)

### 2-1. Analog Output configuration.

MDA-714PC104 has individual DA-converter and analog output circuit for each channel as illustrated in Figure 2-1A. On Direct Output mode, DA-data are written into the DA-converter of each channel directly. They are updated individually or simultaneously with the software command.

On Paced Update mode, DA-data are automatically read out by the Pacer Clock from FIFO memory to each DA-converter, and updated simultaneously

Figure 2-1A. Functional Block

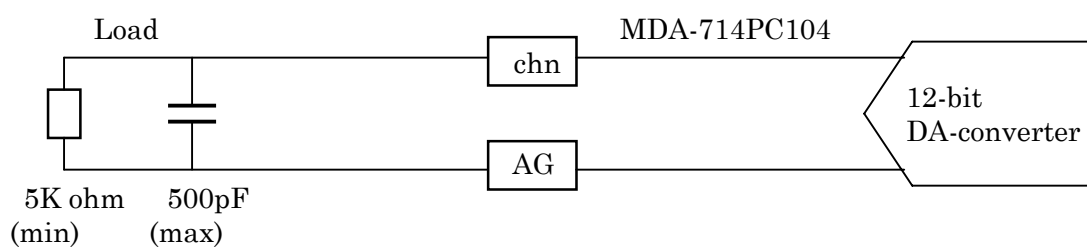


### Drive-ability.

Each Analog Output can drive 5K ohm and 500pF load. Be careful for the capacity of the cable, load over 500pF cause trouble with un-stable output voltage.

Note, twisted-pair or sealed cable has 50-70pF for each meter.

Figure 2-1B.



## 2-2. Analog Output Range

Analog Output Range is selectable with the software command from 0 to +10v, 0 to +5v, -10v to +10v, or -5v to +5v.

The relation between DA-data and Analog Output voltage is follows.

### Resolution.

$$\text{Res} = \text{Vspan} / 4096 \quad < \text{v/digit} >$$

Where Vspan is the width of the range.

For example, 20v for -10v to +10v range.

### DA-data.

$$\text{Dda} = (\text{Vout} / \text{Res}) \quad \text{for Uni-polar Range.}$$

$$\text{Dda} = (\text{Vout} / \text{Res}) + 2048 \quad \text{for Bi-polar Range.}$$

Where Vout is the Analog Output Voltage.

### Analog Output voltage.

$$\text{Vout} = (\text{Dda} \times \text{Res}) \quad \text{for Uni-polar Range.}$$

$$\text{Vout} = (\text{Dda} - 2048) \times \text{Res} \quad \text{for Bi-polar Range.}$$

Figure 2-2A. Uni-polar Output

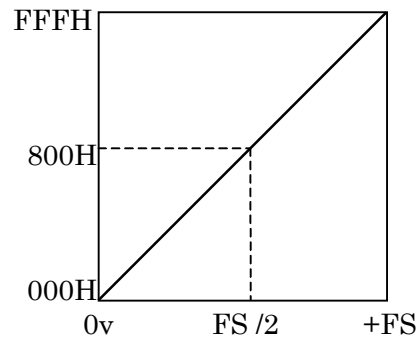


Figure 2-2B. Bi-polar Output

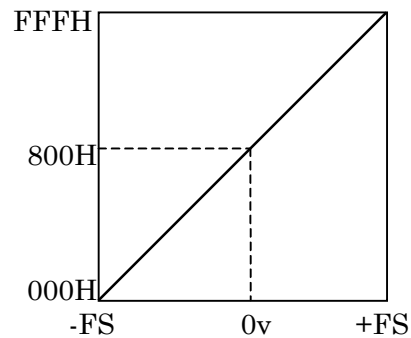


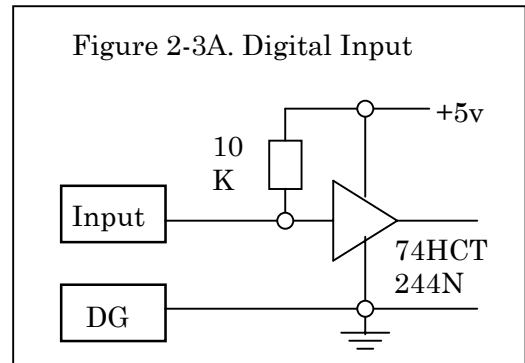
Table 2-2. DA-data vs Analog Output

DA-data	Analog Output <V>			
Hex (Decimal)	-10v to +10v	-5v to +5v	0 to +10v	0 to +5v
FFF (4095)	+9.99512	+4.99756	+9.99756	+4.99878
801 (2049)	+0.00488	+0.00244		
800 (2048)	0.00000	0.00000	+5.00000	+2.50000
7FF(2047)	-0.00488	-0.00244		
001 (0001)	-9.99512	-4.99756	+0.00244	+0.00122
000 (0000)	-10.00000	-5.00000	0.00000	0.00000



## 2-3. Digital Input and Output

All Digital Inputs are TTL level, and pulled-up to +5v with 10K ohm resistor.

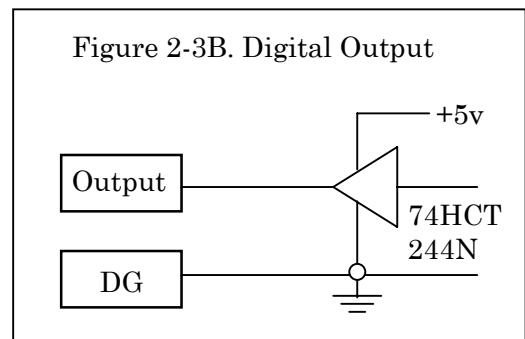


All Digital Outputs are HCT-type CMOS level.

General Purpose Output is latched output, and you can select the logical polarity by on-board switch S-POL.

MICRO SCIENCE set S-POL to "N" as Negative Logic, that cause the output to "CMOS-High" level at power-on reset.

General Purpose Output does not clear by the software reset but clear by power-on hardware reset.





## Section 3. General Programming

### 3-1. General Programming Information

#### Handling

MDA-714PC104 appears to the host PC/104 bus CPU as a block of contiguous 16 hardware registers mapped within the I/O address space.

These registers control the operation of MDA-714PC104 as long as they are accessed using 16bit I/O addressing with each 8bit data transfers.

These registers include Reset-board, Channels of Sampling object, Pacer Clock, Number of Sampling, Triggers, Start/Stop, Interrupt, Status, DA-data, and General Purpose Digital I/O.

#### Operation

MDA-714PC104 does the buffering with on-board FIFO memory, and sampling output automatically.

It is necessary that the program provides the commands and parameters for the operation.

These are explained in order as follows.

( section 3-2 )

General sampling sequences in Manual Update Mode and Paced Update Mode.

( section 3-3 )

Trigger works as a start for Paced Update Operation.

( section 3-4 )

Very useful on-board FIFO buffer memory for seamless Paced Update operation.

( section 3-5 to 3-17 )

The functions of each register. These are the elements for programming.

### 3-2. General Sampling Sequence

MDA-714PC104 has 3 kind of operation Mode.  
They are Direct Update, Paced Cycle Update,  
and Paced Non-Cycle Update mode.  
See follows for detail.

#### 3-2-1. Analog Output Process

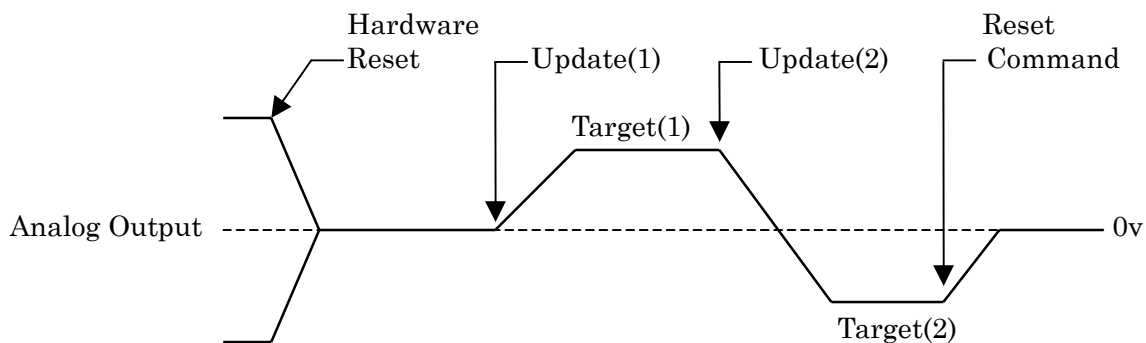
##### Reset Operation.

All Analog Outputs shall return to 0v on  
Reset Command or Hardware Reset  
process.

##### Update Process

On Update operation, Analog Output shall  
change to the new target value(=voltage) at  
a speed of 5v a micro-second, then be in  
stable 0.1% of Full-Scale within 8 micro-  
second on 100pF load for 10v swing.  
This is the **Settling Time**

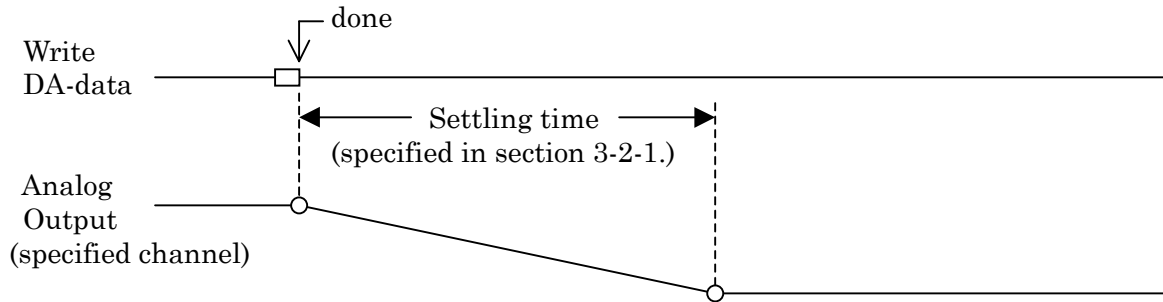
Figure 3-1A. Reset and Update process.



### 3-2-2. Individual Direct Update operation.

In this mode, each Analog Output shall be updated individually with the software command.  
See section 3-7 and 3-15 for programming.

Figure 3-2-2. Update a Channel.



#### Procedure.

```
Rst = inp (BASE+0xF) ; /* Reset the Board, "Rst" is a dummy */
Outp (BASE+0x4, 0x0) ; /* set mode to individually direct, see section 3-7. */
Outp (BASE+0x5, rng) ; /* set output range, see section 3-7. */
```

Then,

```
Outp (BASE+0x0, ch0-L) ; /* Lower byte data for Channel-0 */
Outp (BASE+0x0, ch0-U) ; /* Upper byte data for Channel-0 */
```

Or,

```
Outp (BASE+0x1, ch1-L) ; /* Lower byte data for Channel-1 */
Outp (BASE+0x1, ch1-U) ; /* Upper byte data for Channel-1 */
```

Or,

```
Outp (BASE+0x2, ch2-L) ; /* Lower byte data for Channel-2 */
Outp (BASE+0x2, ch2-U) ; /* Upper byte data for Channel-2 */
```

Or,

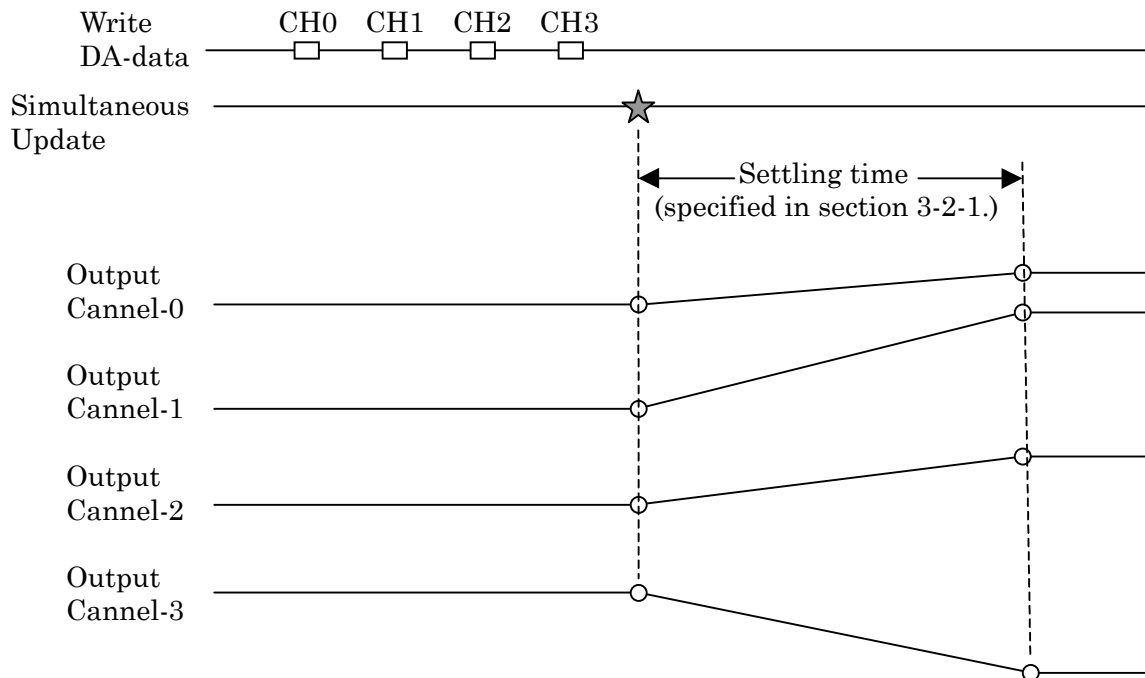
```
Outp (BASE+0x3, ch3-L) ; /* Lower byte data for Channel-3 */
Outp (BASE+0x3, ch3-U) ; /* Upper byte data for Channel-3 */
```

<Note> Write lower byte first then upper byte sequentially,  
and Analog Output word data on DA-converter shall be  
updated at the written timing of upper byte.

**3-2-3. Simultaneous Direct Update operation.**

In this mode, all Analog Output shall be updated simultaneously with the software command.  
See section 3-7 and 3-15 for programming.

Figure 3-2-3. Simultaneous Update all Channels.

**Procedure.**

```
Rst = inp (BASE+0xF) ; /* Reset the Board, "Rst" is a dummy */
Outp (BASE+0x4, 0x20) ; /* set mode to simultaneous direct, see section 3-7. */
Outp (BASE+0x5, rng) ; /* set output range, see section 3-7. */
```

Then,

```
Outp (BASE+0x0, ch0-L) ; /* Lower byte data for Channel-0 */
Outp (BASE+0x0, ch0-U) ; /* Upper byte data for Channel-0 */
Outp (BASE+0x1, ch1-L) ; /* Lower byte data for Channel-1 */
Outp (BASE+0x1, ch1-U) ; /* Upper byte data for Channel-1 */
Outp (BASE+0x2, ch2-L) ; /* Lower byte data for Channel-2 */
Outp (BASE+0x2, ch2-U) ; /* Upper byte data for Channel-2 */
Outp (BASE+0x3, ch3-L) ; /* Lower byte data for Channel-3 */
Outp (BASE+0x3, ch3-U) ; /* Upper byte data for Channel-3 */
```

Finally,

```
Upd = inp (BASE+0xB) ; /* Simultaneous Update, "upd" is a dummy */
```

<Note> Write lower byte first then upper byte sequentially for all Channels, and all Analog Output word data on each DA-converter shall be updated simultaneously at the written timing of update command.

### 3-2-4. Paced Update operation.

Specified Analog Output channels shall be updated simultaneously by the Pacer Clock with the DA-data from the FIFO memory.

#### Paced Cycle Update.

In this mode, on-board FIFO memory works as an endless ring buffer.

Pre-stored one cycle length sequential block DA-data in FIFO memory shall be updated by the Pacer Clock repeatedly for specified times or until Stop Command

#### Paced Non-Cycle Update.

In this mode, on-board FIFO memory works like a pipeline.

DA-converters are updated by the Pacer Clock with the sequential data from the FIFO memory for specified times or until Stop Command.

Additional data can be written into the FIFO memory until it become Full.

Not-Full or Not-Half-Full state flag is useful for the trigger to write additional data.

#### Procedure.

```

Rst = inp (BASE+0xF) ; /* Reset the Board, "Rst" is a dummy */
Outp (BASE+0x4, mode) ; /* set mode to paced update, see section 3-7. */
Outp (BASE+0x5, rng) ; /* set output range, see section 3-7. */
Outp (BASE+0x6, source) ; /* select Pacer Clock Source, see section 3-8. */
Outp (BASE+0x7, div-0) ; /* set Pacer Clock, see section 3-9. */
Outp (BASE+0x7, div-1) ;
Outp (BASE+0x7, div-2) ;
Outp (BASE+0x7, div-3) ;
Outp (BASE+0x8, num-0) ; /* set Times to Update, see section 3-10. */
Outp (BASE+0x8, num-1) ;
Outp (BASE+0x8, num-2) ;
Outp (BASE+0x8, num-3) ;
Outp (BASE+0x9, Trg) ; /* set output Trigger mode, see section 3-11. */
Outp (BASE+0xA, intr) ; /* set interrupt source if use, see section 3-13. */

for
one
Update → Outp (BASE+0x0, ch0-L) ; /* Lower byte data for Channel-0 */
           Outp (BASE+0x0, ch0-U) ; /* Upper byte data for Channel-0 */
           Outp (BASE+0x0, ch1-L) ; /* Lower byte data for Channel-1 */
           Outp (BASE+0x0, ch1-U) ; /* Upper byte data for Channel-1 */
           Outp (BASE+0x0, ch2-L) ; /* Lower byte data for Channel-2 */
           Outp (BASE+0x0, ch2-U) ; /* Upper byte data for Channel-2 */
           Outp (BASE+0x0, ch3-L) ; /* Lower byte data for Channel-3 */
           Outp (BASE+0x0, ch3-U) ; /* Upper byte data for Channel-3 */

           /* Write sequential data into FIFO memory same as above */

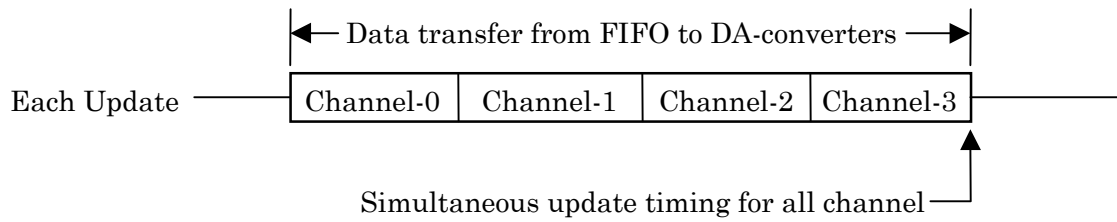
           Outp (BASE+0xB, str) ; /* Start Paced operation on Trigger. */
           Status-1 = inp (BASE+0xC) ; /* Get Status-1, see section 3-13. */
           Status-2 = inp (BASE+0xD) ; /* Get Status-2, see section 3-13. */

           /* Write additional DA-data on Non-Cycle mode */

           Outp (BASE+0xB, stp) ; /* Stop Paced operation, see section 3-12. */

```

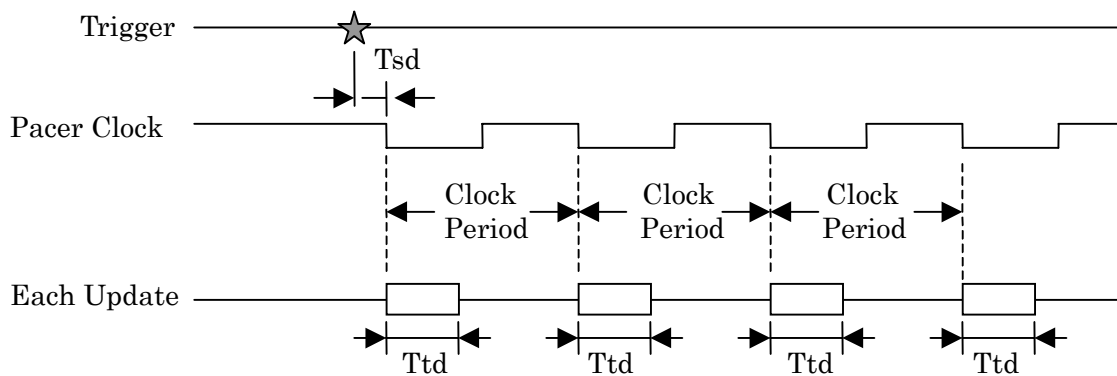
Figure 3-2-4A. One-Scan Update for Paced operation.



<Note-1> Figure 3-2-4A shows for using 4 channels,  
 Channel-0 to 2 for using 3 channels,  
 Channel-0 to 1 for using 2 channels,  
 Channel-0 for using only 1 channel, as same above.

<Note-2> Data transfer time is 500ns a channel

Figure 3-2-4B. Paced operation flow



Where Tsd is Start delay  $\leq 125\text{ns}$  from the Trigger.

Ttd is transfer delay = 2000ns for using 4 channels.

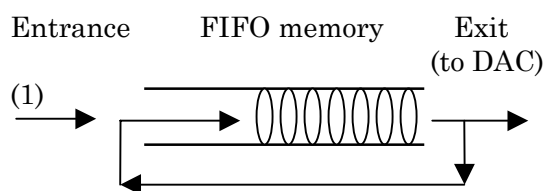
=1500ns for using 3 channels.

=1000ns for using 2 channels.

= 500ns for using only 1 channel.

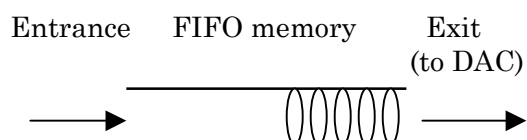
Each Update is simultaneously for all channels.

Figure 3-2-4C. Paced Cycle Update



- (1) Write one cycle length sequential DA-data block.
- (2) After start, the DA-data block shall be re-circulated automatically.

Figure 3-2-4D. Paced Non-Cycle Update



After start, written DA-data flows through the FIFO memory only, not be re-cycled.



### 3-3. Variety of Triggers

The software selected trigger makes the Pacer Clock start or enable.

The variety of triggers allow the board to be adapted to a wide range of applications as follows.

See section 3-11 for the programming.

#### Software Trigger.

You can insert the Software Trigger Command as a immediate start for the Pacer Clock at any time or any point of the application software process.

#### External Digital Edge Trigger.

When External Digital Edge Trigger is enabled, rising or falling edge of External (74HCT-type CMOS) input “TRG-IN” makes the Pacer Clock start.

Figure 3-3A shows the operation, in which as a rising edge of “TRG-IN” for trigger is illustrated at upper side, and a falling edge is at lower side. They are also software selectable as a polarity of “+” or “-”.

#### External Digital Level Trigger.

External (74HCT-type CMOS) input “TRG-IN” can also be useful for the Gated Update that enable the Pacer Clock as long as the software selectable valid level.

Figure 3-3B shows the work of “TRG-IN” in which “valid level=High” for Gate-On is illustrated at upper side, and “valid level=Low” is at lower side.

Note that another Gated Update shall be executed if another “valid level” come as long as Digital Level Trigger is enabled.

Figure 3-3A.  
External Digital Edge Trigger

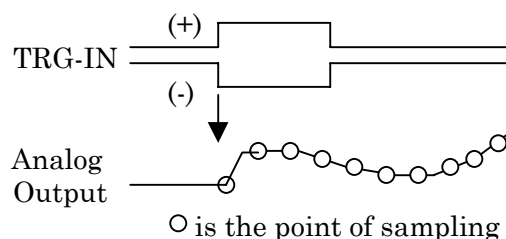
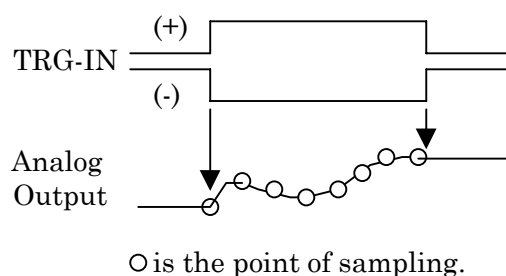


Figure 3-3B.  
External Digital Gated Acquisition



### 3-4. On-Board FIFO Memory

On-Board FIFO buffer memory allows the program asynchronous data write in. The Program is always free from taking care of the hardware timing in data write in process while sampling process is being executed on the board.

MDA-714PC104 provides “Not-Full”, “Not-Half-Full”, and “Data-Lost” flag as the FIFO memory status.

In any time, the program can not only read the Flags for polled method of data write in, but also use them as the trigger for interrupt operation.

Figure 3-4A shows how the FIFO memory works on the board.

The standard model of MDA-714PC104 has 1024 words of data capacity that is enough for many applications.

When the data read out from the FIFO memory, un-occupied area shall be expanded up to the capacity. This feature is very useful when the program need to write the data while sampling process is being executed and or need the unlimited update.

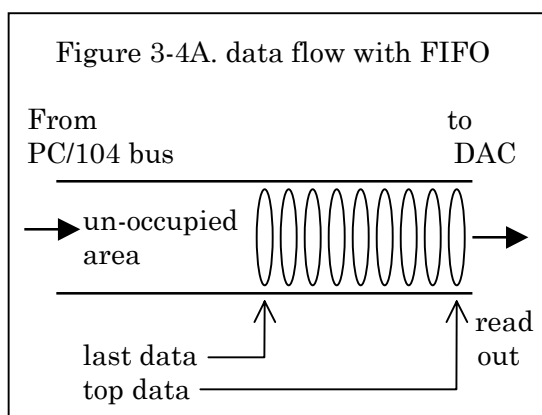


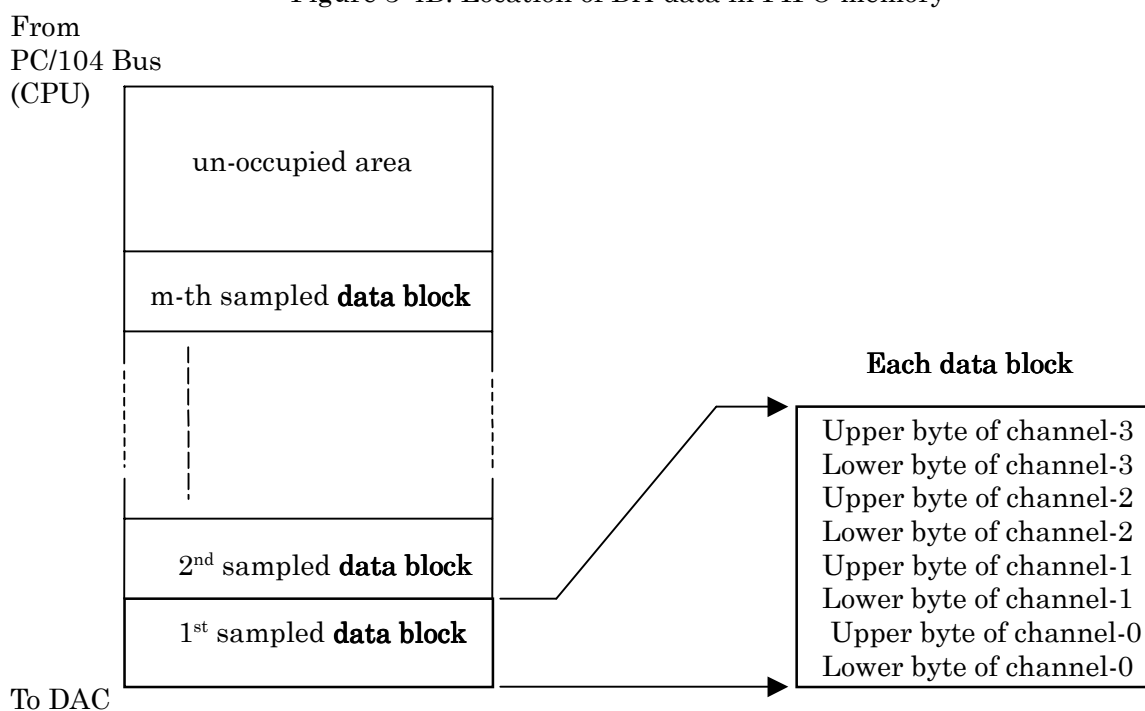
Table 3-4. Status Flag of FIFO memory

item	status
Not-Full	Acceptable one or more.
Not-Half-Full	Occupied grater than half of the capacity.
Data Lost	Borrow was happened.

It is possible to expand the capacity of FIFO memory by replace the device.

8K, 1M, or 8M words is available at the purchase order in option.

Figure 3-4B. Location of DA-data in FIFO memory



### 3-5. I/O Register Memory Map

MDA-714PC104 appears as a 16-byte block of registers within the host CPU's I/O address space. This address block must not conflict with other system I/O devices.

You can program the on-board switches SW1, SW2, and SW3 as BASE ADDRESS of the board.

These hex-a-decimal defined switches are set to SW1=0, SW2=1, SW3=E at the factory of MICRO SCIENCE, that specify the BASE ADDRESS to "01E0" hex.

MDA-714PC104 occupies upper 16 byte address from the BASE.

See figure 1-4 for the location of the board.

Figure 1-5A. Setting the BASE ADDRESS




Address Line →	AB15 to AB12	AB11 to AB08	AB07 to AB04	AB03 to AB00
On-board Hex-a-decimal → Switches				on-board logic decoded for multiple ports
Factory setting →	0	1	E	( F to 0 )

Table 3-5. MDA-714PC104 Register Assignment. (All the port consist of 8bit.)

I/O Address	Direction	Description	Refer to
BASE +FH	Read	Reset Board, and get ID.	Section 3-6
	Write		
BASE +EH	Read	External Control Elements Input state.	Section 3-19
	Write	General Purpose Digital Output. (latched)	
BASE +DH	Read	2ndary Status.	Section 3-14
	Write	Clear 2ndary Status.	
BASE +CH	Read	Primary Status.	
	Write	Clear Primary Status.	
BASE +BH	Read	Simultaneous Manual Update	Section 3-15
	Write	Start or Stop for Paced Update	Section 3-12
BASE +AH	Read		
	Write	Interrupt Source or State.	Section 3-13
BASE +9H	Read		
	Write	Trigger Source and Mode	Section 3-11
BASE +8H	Read	Paced Operation Counter.	Section 3-10
	Write		
BASE +7H	Read		
	Write	Divide Ratio to the Pacer Clock Source.	Section 3-9
BASE +6H	Read		
	Write	Pacer Clock Source.	Section 3-8
BASE +5H	Read		
	Write	Analog Output Range	Section 3-7
BASE +4H	Read		
	Write	Analog Output Mode and Channels	Section 3-7
BASE +3H	Read		
	Write	Write DA-data to Channel-3 direct	Section 3-15
BASE +2H	Read		
	Write	Write DA-data to Channel-2 direct	Section 3-15
BASE +1H	Read		
	Write	Write DA-data to Channel-1 direct	Section 3-15
BASE +0H	Read		
	Write	Write DA-data to FIFO / to Channel-0 direct	Section 3-15

## 3-6. Reset the Board, and get ID

```
rst = inp (BASE+0xF) ; /* Reset the Board */
```

Read (BASE+FH) Register cause the board reset.

All registers of the board must be initialized except for the last values of General Purpose Digital Output described in section 3-17.

The Paced Update process shall be broken, and previous DA-data in the FIFO memory must be lost.

Where “rst” is the ID that depend on the board, “1EH” for MDA-714PC104.

Table 3-6. Read (BASE+FH) Register Bit Field.

Bit	Description
B7	1EH is the ID for MDA-714PC104.
B6	
B5	
B4	
B3	
B2	
B1	
B0	

## 3-7. Analog Output Mode, Channels, Range

Set Mode and Channels

outp (BASE+0x4, mc) ; /\* Mode and Channels selection \*/

Write (BASE+4H) Register specifies the Mode and channels for Analog Outputs.

## &lt;Note-1&gt;

From Analog Output Channel-0 to the specified final channel-n shall be operated in Paced Update Mode.

Table 3-7B shows the structure of the bit field for specifies “n”.

DA-data shall be transferred from FIFO memory to each DA-converter synchronously with the Pacer Clock.

## &lt;Note-2&gt;

DA-data should be written directly to each DA-converter with the Write Command. Analog Output Update timing is specified by the Bit “B5” on Immediate Update mode. See section 3-2 for the procedure.

Table 3-7A. Write (BASE+4H) Register Bit Field.

Bit	Term	“=1” specifies	“=0” specifies	on Reset
B7 B6	Not used.			0 0
B5	Timing on Immediate Update mode	Simultaneous	Individual	0
B4	Analog Output Mode	Paced Update	Immediate	0
B3 B2	Not used.			0 0
B1 B0	Final Channel of each Sampling-Scan on Paced Update mode. <Note-1>	See Table 3-7B		0 0

Table 3-7B

B1	B0	Final Channel Number
1	1	3
1	0	2
0	1	1
0	0	0

Table 3-7C

B5	B4	Operation Mode
1	1	Paced Update <Note-3>
1	0	Simultaneous Immediate Update
0	1	Paced Update <Note-3>
0	0	Individual Immediate Update

<Note-3> Update timing is Simultaneous on Paced Update mode.

## Set Analog Output Range

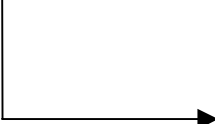
```
outp (BASE+0x5, rng) ; /* Analog Output Range */
```

Write (BASE+5H) Register specifies  
the Analog Output Range for each channel  
individually.

Table 3-7D. Write (BASE+5H) Register Bit Field.

Bit	Code	Term	on Reset
B7	R1	Analog Output Range for Channel-3	0
B6	R0		0
B5	R1	Analog Output Range for Channel-2	0
B4	R0		0
B3	R1	Analog Output Range for Channel-1	0
B2	R0		0
B1	R1	Analog Output Range for Channel-0	0
B0	R0		0

Table 3-7E



R1	R0	Analog Output Range
1	1	-5v to +5v
1	0	-10v to +10v
0	1	0v to +5v
0	0	0v to +10v

<Note-4> Analog Output Range shall be updated  
when DA-data updated simultaneously.

## 3-8. Pacer Clock Source Selection

outp (BASE+0x6, cks) ; /\* Clock Source \*/

Write (BASE+6H) Register specifies the Pacer Clock Source that should be divided to generate the Pacer Clock.  
Table 3-8 shows the structure of the bit field.  
The bit “B4” select the Pacer Clock Source either Internal or External of the board.

The bit “B7” select the valid edge of the External Clock Source.  
Where, External Clock Source Input “CLK-IN” must be TTL level, and the frequency is less than 10MHz.  
Internal Clock Source is 20MHz.

Table 3-8. Write (BASE+6H) Register Bit Field.

Bit	Term	=”1” specifies	=”0” specifies	on Reset
B7	Select the valid edge of “CLK-IN”	Rising edge (+)	falling edge (-)	0
B6	Not used			0
B5				0
B4	Select the Pacer Clock Source	External “CLK-IN”	Internal	0
B3	Not used			0
B2				0
B1				0
B0				0

<Note>

External Clock Source must be less than 10MHz,  
and both state of the level must be longer than  
45 ns.

## 3-9. Divide Ratio to Pacer Clock Source

outp (BASE+0x7, div0) ; /\* 1<sup>st</sup> data = Least significant byte of divide ratio \*/  
 outp (BASE+0x7, div1) ; /\* 2<sup>nd</sup> data = 3<sup>rd</sup> significant byte of divide ratio \*/  
 outp (BASE+0x7, div2) ; /\* 3<sup>rd</sup> data = 2<sup>nd</sup> significant byte of divide ratio \*/  
 outp (BASE+0x7, div3) ; /\* 4<sup>th</sup> data = Most significant byte of divide ratio \*/

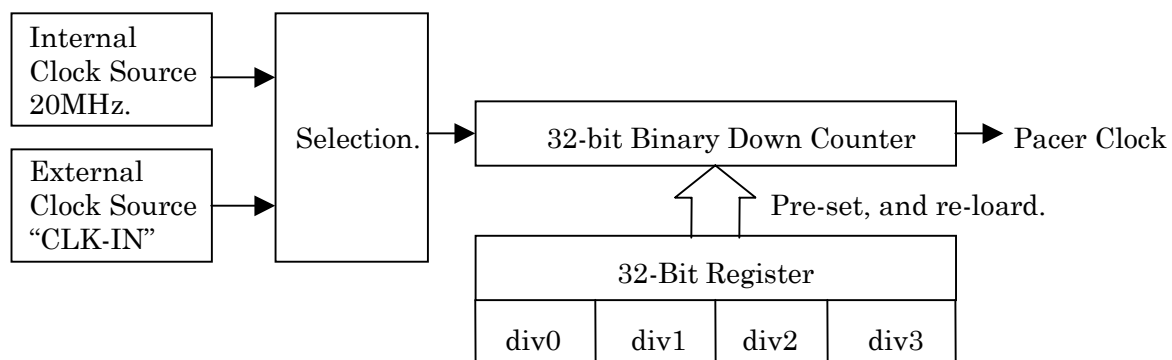
Write (BASE+7H) Register specifies the divide ratio to the Pacer Clock Source that specifies the Pacer Clock.  
 Single 32-bit binary counter must be written as 4-byte data in order as describe above.

They are held in the same bit-wide registers and automatically re-load the counter at reaching “0” by down-counting as a divider.  
 Figure 3-9 shows the configuration of generating Pacer Clock.

Table 3-9. Write (BASE+7H) Register Bit Field.

Bit	1 <sup>st</sup> data (div0)	2 <sup>nd</sup> data (div1)	3 <sup>rd</sup> data (div2)	4 <sup>th</sup> data (div3)	on Reset
B7	Least significant byte of divide ratio.	3 <sup>rd</sup> significant byte of divide ratio.	2 <sup>nd</sup> significant byte of divide ratio.	Most Significant byte of divide ratio.	0
B6					0
B5					0
B4					0
B3					0
B2					0
B1					0
B0					0

Figure 3-9. Configuration of generating Pacer Clock.





### 3-10. Paced Operation Counter

The number of Update should be specified with the counter on Limited Paced Update mode. Other hand, this counter does not work on Un-Limited Paced Update mode. You can also specify either Cycle mode or Non-Cycle mode. See section 3-12 for details.

#### (1) on Limited Paced Non-Cycle Update mode

```
outp (BASE+0x8, num0); /* 1st data = Least Significant byte */
outp (BASE+0x8, num1); /* 2nd data = 3rd Significant byte */
outp (BASE+0x8, num2); /* 3rd data = 2nd Significant byte */
outp (BASE+0x8, num3); /* 4th data = Most Significant byte */
```

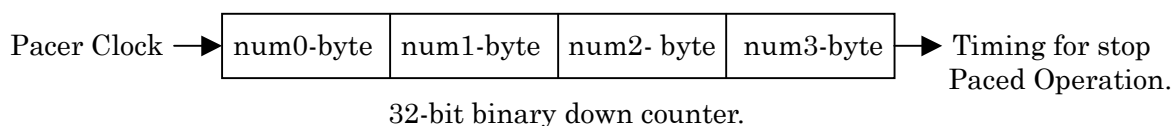
Write (BASE+8H) Register specifies the Number of Update with the Pacer Clock. 32-bit binary pre-settable down counter must be written as 4-byte data in order as described above.

This Paced Operation Counter shall being count down by the Pacer Clock until decreased to "0". Figure 3-10A shows the configuration of Paced Operation Counter.

Table 3-10A. Write (BASE+8H) Register Bit Field on **Non-Cycle mode**.

Bit	1 <sup>st</sup> data (num0)	2 <sup>nd</sup> data (num1)	3 <sup>rd</sup> data (num2)	4 <sup>th</sup> data (num3)	on Reset
B7	Least significant byte.	3 <sup>rd</sup> significant byte.	2 <sup>nd</sup> significant byte.	Most Significant byte.	0
B6					0
B5					0
B4					0
B3					0
B2					0
B1					0
B0					0

Figure 3-10A. Paced Operation Counter on **Non-Cycle mode**.



The program can also read out the Paced Operation Counter as a rest of the Updates.

This 32-bit binary counter must be read as 4-byte data in order as described below.

Read out

```
Num0 = inp (BASE+0x8); /* 1st data = Least Significant byte */
Num1 = inp (BASE+0x8); /* 2nd data = 3rd Significant byte */
Num2 = inp (BASE+0x8); /* 3rd data = 2nd Significant byte */
Num3 = inp (BASE+0x8); /* 4th data = Most Significant byte */
```

## (2) on Limited Paced Cycle Update mode

```

outp (BASE+0x8, pnt0) ; /* 1st data = Lower byte of number of point */
outp (BASE+0x8, pnt1) ; /* 2nd data =Upper byte of number of point */
outp (BASE+0x8, tms0) ; /* 3rd data = Lower byte of repeat times */
outp (BASE+0x8, tms1) ; /* 4th data = Upper byte of repeat times */

```

Write (BASE+8H) Register specifies the Number of Update with the Pacer Clock. 32-bit binary pre-settable down counter must be written as 4-byte data in order as described above.

Analog wave form cycle data that consists of the “number of point” should be written in the on-board FIFO memory before start Paced Update operation.

Point Counter shall being count down to “0”, and re-load then count down to “0” with the Pacer Clock repeat until Times Counter decrease to “0”

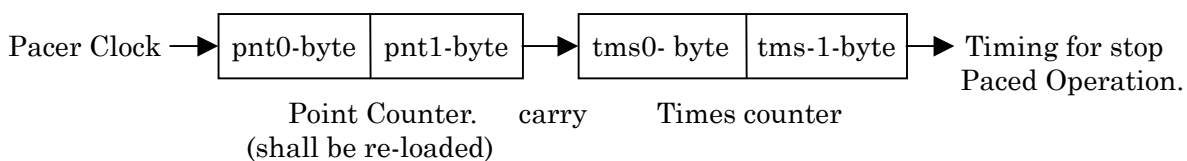
Times Counter shall being count down decreased to “0” by the carry of Point Counter.

Figure 3-10B shows the configuration of Paced Operation Counter in Cycle mode.

Table 3-10B. Write (BASE+8H) Register Bit Field on **Cycle mode**.

Bit	1 <sup>st</sup> data (pnt0)	2 <sup>nd</sup> data (pnt1)	3 <sup>rd</sup> data (tms0)	4 <sup>th</sup> data (tms1)	on Reset
B7					0
B6					0
B5					0
B4	Lower byte of	Upper byte of	Lower byte of	Upper byte of	0
B3	number of point	number of point	repeat times for	repeat times for	0
B2	in one cycle.	in one cycle.	the cycle data.	the cycle data.	0
B1					0
B0					0

Figure 3-10B. Paced Operation Counter on **Cycle mode**.



The program can also read out the Paced Operation Counter as a rest of the Updates. This 32-bit binary counter must be read as 4-byte data in order as described below.

“**Rest point**” is the rest number of point in current cycle.

“**Rest times**” is the rest number of times to be repeated the cycle.

#### Read out

```

Pnt0 = inp (BASE+0x8) ; /* 1st data = Lower byte of Rest point */
Pnt1 = inp (BASE+0x8) ; /* 2nd data = Upper byte of Rest point */
Tms0 = inp (BASE+0x8) ; /* 3rd data = Lower byte of Rest times */
Tms1 = inp (BASE+0x8) ; /* 4th data = Upper byte of Rest times */

```

## 3-11. Trigger Source and Mode

```
outp (BASE+0x9, tgm) ; /* Trigger Source and Mode */
```

Write (BASE+9H) Register specifies the Trigger Mode, Source, and Polarity for the Paced Update.

Bit “B3” specifies the Digital Trigger Mode.

Bit “B4” specifies the Polarity of the Digital Trigger.

Bit “B6” specifies to enable or disable the Digital Trigger.

Bit “B7” specifies to enable or disable the Software Trigger.

Table 3-11A. Write (BASE+9H) Register Bit Field.

Bit	Term	“=1” specifies	“=0” specifies	on Reset
B7	Software Trigger.	Enable	Disable	0
B6	External Digital Trigger.	Enable	Disable	0
B5	Not used.			0
B4	Polarity of Digital Trigger.	+ (or Rising Edge)	- (or Falling Edge)	0
B3	Digital Trigger Mode	Edge	Level	0
B2	Not used.			0
B1				0
B0				0

## &lt;On and OFF the Paced Update operation&gt;

Start Command that specified in the next section 3-12 cause MDA-714PC104 into waiting Trigger state, then Paced Update operation shall be started on detecting any Trigger that enabled, and stopped on the counter decrease to “0” on Limited Paced Update Mode. Stop Command that specified in the next section 3-12 also cause to stop the Paced operation in any mode.

## &lt;Multi Trigger Source&gt;

Because both Trigger Sources are enabled or disabled individually, they work like the switches connected in parallel.

## &lt;Delay to Start&gt;

The delay time to start Paced Update operation with the Internal Clock Source from detect the Trigger is specified as follows.

On Software Trigger; 375ns (max),

On External Digital Trigger ; 405ns (max),

Other hand with the External Clock Source, plus 1 Clock Source Period to that value.

## &lt;Example&gt;

The procedure of Start Paced Update operation with the software Trigger is follows.

(1)

Write (BASE+9H) Register to Bit “B7”=1, then Write (BASE+BH) as a Start Command.

or(2)

Write (BASE+BH) as a waiting for Trigger Start Command, then Write (BASE+9H) Register to Bit “B7”=1 as a immediate Trigger.

## &lt;Gated Update&gt;

External Digital Level Trigger works as a Gated Update operation that enabled Write (BASE+9H) Register to Bit “B6”=1, “B3”=0, and specify the Polarity with “B4”. Paced Update operation shall be executed among the specified Level.

----- How the Trigger works for Paced Update operation -----

Specified Trigger operate with the Start Command for the post trigger Paced operation as illustrated in Figure 3-11A,B,C. Although these are illustrated as after Start Command, it is also valid that specify the Trigger before Start Command.

Where ▼ is the start-timing, ▽ is the stop-timing for Paced operation.

Paced operation shall be stopped by Stop Command or the counter decrease to "0" on the Limited Update mode.

Figure 3-11A. With the Software Trigger.

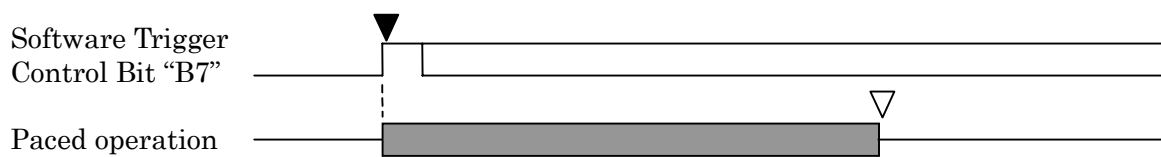
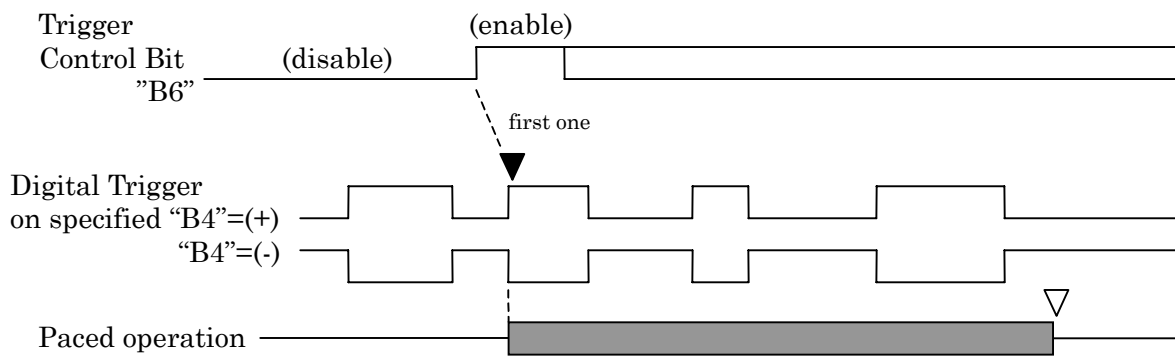


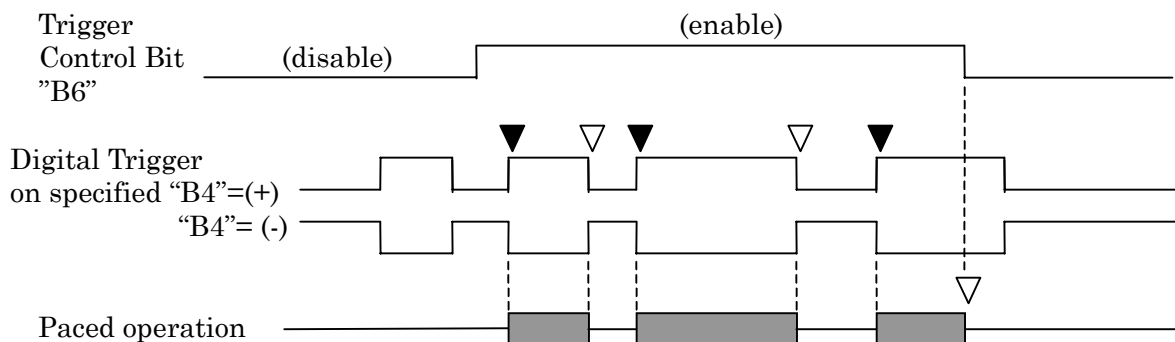
Figure 3-11B. With the Digital Edge Trigger.



<Note> After Enable and Start Command, the first valid Edge of "TRG-IN" is the Trigger.

Trigger Mode specify Bits must be set to "B3"=1 as a edge mode.

Figure 3-11C. With the Digital Level Trigger.



<Note> Trigger Mode specify Bits must be set to "B3"=0 as a level mode.

## 3-12. Start / Stop Paced operation

out (BASE+0xB, str) ; /\* Control the Paced Operation \*/

Write (BASE+BH) Register specifies the Paced operation Mode, and ON/OFF control. Bit “**B7**” specifies the Paced operation whether Paced Update or only Pacer Clock run.

Bit “**B2**” specifies the Paced operation whether Cycle mode or Non-Cycle through mode for on-board FIFO memory.

Bit “**B1**” specifies the Paced operation whether Un-Limited run until “Stop” or Limited run with the counter that is specified in section 3-10.

Bit “**B0**” controls Start and Stop the Paced operation.

Where “Start” means “waiting for Trigger” that is a post Trigger operation.

MDA-714PC104 is waiting for the Trigger to start the Paced operation by set “B0”=1, and shall be stopped by set “B0”=0.

Table 3-12A. Write (BASE+BH) Register Bit Field.

Bit	Term	“=1” specifies	“=0” specifies	on Reset
B7	Paced Operation	Pacer Clock only	Paced Update	0
B6	Not used			0
B5				0
B4				0
B3				0
B2	Cycle / Non-Cycle operation.	Cycle	Non-Cycle	
B1	Limited / Un-Limited operation.	Limited by counter	Endless	0
B0	Start / Stop Command	Start	Stop	0

1) **Un-Limited run.**

This Command cause MDA-714PC104 into waiting for Trigger to start Un-Limited Paced Update operation that shall run until put “Stop” Command.

(2) **Limited run.**

This Command cause MDA-714PC104 into waiting for Trigger to start Limited Paced operation that shall run until count down to “0” of the counter or put “Stop” Command.

(3) **Un-Limited run only Pacer Clock.**

This Command cause MDA-714PC104 into waiting for Trigger to start Un-Limited run only Pacer Clock until put “Stop” Command.

(4) **Limited run only Pacer Clock.**

This Command cause MDA-714PC104 into waiting for Trigger to start Limited run only Pacer Clock until count down to “0” of the counter or put “Stop” Command.

<Note> **Re-Start.**

“Stop” command must be put before re-start Paced operation in case of stopped by the counter.

Table 3-12B. Bit pattern to control the Paced Operation.

B7	B2	B1	B0	(start on trigger) Operation
1	1	1	1	Pacer Clock only, Limited Cycle run until “counter”=0, or “Stop”.
1	1	1	0	Stop
1	1	0	1	Pacer Clock only, Un-Limited Cycle run until “Stop”.
1	1	0	0	Stop
1	0	1	1	Pacer Clock only, Limited Non-Cycle run until “counter”=0, or “Stop”.
1	0	1	0	Stop
1	0	0	1	Pacer Clock only, Un-Limited Non-Cycle run until “Stop”.
1	0	0	0	Stop
0	1	1	1	Limited Paced Cycle Update until “counter”=0, or “Stop”.
0	1	1	0	Stop
0	1	0	1	Un-Limited Paced Cycle Update until “Stop”.
0	1	0	0	Stop
0	0	1	1	Limited Paced Non-Cycle Update until “counter”=0, or “Stop”.
0	0	1	0	Stop
0	0	0	1	Un-Limited Paced Non-Cycle Update until “Stop”.
0	0	0	0	Stop

## 3-13. Interrupt Source Selection

```
outp (BASE+0xA, isd ) ; /* Interrupt Source */
```

Write (BASE+AH) Register specifies enable or disable individual Interrupt Source. Hardware state in the MDA-714PC104 that is enabled shall cause an interrupt request to the host CPU.

Interrupt request may be used to synchronize the transfer of DA-data to MDA-714PC104 or something.

Interrupt Level is selected by the jumper switch “JP-INT” illustrated in Figure 1-5B.

Table 3-13A. Select the Interrupt Level.

“JP-INT”	Level
IRQ 3	3
IRQ 4	4
IRQ 5	5
IRQ 6	6
IRQ 7	7
IRQ 9	9
NC	Non-use

Table 3-13B. Write (BASE+AH) Register Bit Field

Bit	Interrupt Timing	“=0” specifies	“=0” specifies	On Reset
B7	Valid edge of Digital Input “INT-IN”	+ (rising edge)	- (falling edge)	0
B6	“Half-Full” state of FIFO memory	Enable	Disable	0
B5	“Not-Full” state of FIFO memory	Enable	Disable	0
B4	The End of the Paced operation	Enable	Disable	0
B3	Initial timing of every Cycle	Enable	Disable	0
B2	Detected the Trigger	Enable	Disable	0
B1	Digital Input “INT-IN”	Enable	Disable	0
B0	Initial edge of every Pacer Clock	Enable	Disable	0

Bit “**B7**” specify the valid edge of Digital Input “INT-IN” If it enabled.

Bit “**B6**” to “**B0**” specify that enable or disable of each Interrupt Source.

Bit “**B4**” specify that enable or disable to interrupt by the counter decrease to “0” on Limited Paced Operation. Note, Stop Command doesn’t work for the Interrupt.

Bit “**B3**” control the interrupt source of the Initial-Timing of every Cycle in Paced Cycle operation.

It shall be appear “m” times among the Limited operation, where “m” is the number that written to the Paced operation counter specified as section 3-10.

## 3-14. Board Status

```
sts1 = inp (BASE+0xC) ; /* Primary Status */
sts2 = inp (BASE+0xD) ; /* Secondary Status */
```

Read (BASE+CH) and (BASE+DH) Register provides the Status of the Board, and allows the host CPU to watch the operation process in real time.

Table 3-14A. Read (BASE+CH) Register Bit Field

Bit	Term	"=1" specifies	"=0" specifies	On Reset
B7	End of the Paced operation <Note1>	Complete	Not-Complete	0
B6	Initial of the Cycle <Note1>	Occurred	Not-Occurred	0
B5	Not used.			0
B4	Over-run Error <Note1>	Occurred	Not-Occurred	0
B3	(FIFO) Data Lost Error <Note1>	Occurred	Not-Occurred	0
B2	(FIFO) Not-Full <Note2>	Not-Full	Full	0
B1	(FIFO) Not-Half-Full <Note2>	Not-Half-Full	Up-Half-Full	0
B0	(FIFO) Not-Empty <Note2>	Not-Empty	Empty	0

&lt;Note1&gt;

Bit "B7" "B6" "B4" "B3" are the latched flags that held the status until reset by the Board Reset, or Write (BASE+CH) Register with the clear command.

&lt;Note2&gt;

Bit "B2" "B1" "B0" are the state flags that shall be automatically change with the state of the Paced operation process.

Bit "B7" shall be set when the counter decrease to "0" that means the Limited Paced operation is complete.

Note, it must not be set by the Stop Command.

Bit "B6" shall be set when the initial of every Cycle in Cycle operation. See section 3-12 for details of the Cycle operation.

Bit "B4" shall be set when too much high frequency clock applied as a Pacer Clock.

Bit "B3" shall be set when get the fault in Paced Update operation, because empty of the FIFO memory.

Bit "B2" is the Not-Full state flag that indicates the number of data in the FIFO memory is less than a full state.

Bit "B1" is the Not-Half-Full state flag that indicates the number of data in the FIFO memory is less than or equal to a half of its capacity.

Bit "B1=0" means the number of data in FIFO memory is greater than a half of its capacity.

This is very useful for fast block data transfers that should be executed by CPU command with polled status.

Bit "B0" is the Not-Empty state flag that indicates the number of data in the FIFO memory is greater than or equal to one.



Table 3-14B. Read (BASE+DH) Register Bit Field

Bit	Term	"=1" specifies	"=0" specifies	On Reset
B7	Not used.			0
B6				0
B5				0
B4				0
B3				0
B2	Interrupt Request <Note1>	Applied	Not-Applied	0
B1	Initial edge of every Pacer Clock <Note1>	Applied	Not-Applied	0
B0	Trigger <Note1>	Applied	Not-Applied	0

&lt;Note1&gt;

Bit "B2" "B1" "B0" are the latched flags that held the status until reset by the Board Reset, or Write (BASE+DH) Register with the clear command.

Bit "**B2**" shall be set when the interrupt request applied.

Bit "**B1**" shall be set when the valid edge of Pacer Clock applied.

Bit "**B0**" shall be set when the valid Trigger applied. This Bit shall be reset not only by the Board Reset or Write (BASE+DH) Register with the clear command, but also by Write (BASE+9H) Register as the Trigger source and mode selection.

## Clear Status

```

outp (BASE+0xC, stc1 ) ; /* Clear Status 1 */
outp (BASE+0xD, stc2 ) ; /* Clear Status 2 */

```

Write (BASE+CH) and (BASE+DH) Register work for reset flags individually.

Table 3-14C. Write (BASE+CH) Register Bit Field

Bit	Term	"=1" specifies	"=0" specifies	On Reset
B7	for End of the Paced operation flag	Clear	Non-effect	0
B6	for Initial of the Cycle flag	Clear	Non-effect	0
B5				0
B4	for Over-run Error flag	Clear	Non-effect	0
B3	for (FIFO) Data Lost Error flag	Clear	Non-effect	0
B2	Not used			0
B1	Not used			0
B0	for all of FIFO memory	Clear	Non-effect	0

Bit "**B0=1**" works to clear the FIFO memory, not only their status but also stored data same as the Board Reset.

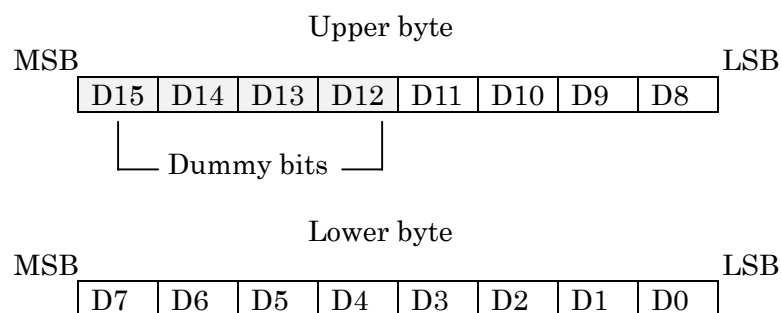
Table 3-14D. Write (BASE+DH) Register Bit Field

Bit	Term	"=1" specifies	"=0" specifies	On Reset
B7	Not used.			0
B6				0
B5				0
B4				0
B3				0
B2	for Interrupt Request flag	Clear	Non-effect	0
B1	for Initial edge of every Pacer Clock flag	Clear	Non-effect	0
B0	for Trigger flag	Clear	Non-effect	0

## 3-15. Write DA-data

One 12-bits DA-data consists of upper 4-bits and lower 8-bits. They should be written as two byte data. Upper 4-bits of the upper byte are ignored as dummy.

The code of the data is straight-binary for uni-polar output range, or offset-binary for bi-polar output range.



Direct Update operation

 (skip FIFO)
**Individual Immediate Direct Update.**

Write lower byte first, then follow upper byte to any channel address, and latch of the DA-converter shall be updated at the timing of writing upper byte.

**Simultaneous Direct Update.**

Write DA-data from Channel-0 to N as same as individual immediate direct update, then finally, Write (BASE+0xB) Register as a simultaneous update command.

Prepare,

```
Rst = inp (BASE+0xF) ; /* Reset the Board, "Rst" is a dummy */
Outp (BASE+0x4, mode) ; /* Individual or Simultaneous, see section 3-7. */
Outp (BASE+0x5, rng) ; /* Analog Output Range, see section 3-7. */
```

Then,

```
Outp (BASE+0x0, ch0-L) ; /* Lower byte data for Channel-0 */
Outp (BASE+0x0, ch0-U) ; /* Upper byte data for Channel-0 */
Outp (BASE+0x1, ch1-L) ; /* Lower byte data for Channel-1 */
Outp (BASE+0x1, ch1-U) ; /* Upper byte data for Channel-1 */
Outp (BASE+0x2, ch2-L) ; /* Lower byte data for Channel-2 */
Outp (BASE+0x2, ch2-U) ; /* Upper byte data for Channel-2 */
Outp (BASE+0x3, ch3-L) ; /* Lower byte data for Channel-3 */
Outp (BASE+0x3, ch3-U) ; /* Upper byte data for Channel-3 */
```

In case for Simultaneous update mode,

Finally,

```
Upd = inp (BASE+0xB) ; /* Simultaneous Update, "upd" is a dummy */
```

<Note> See section 3-2 for more information.

### Paced Update operation (into FIFO)

Write lower byte first, then follow upper byte from Channel-0 to N sequentially into FIFO memory as a block of data for one update.

Write any blocks of data sequentially within the capacity of the FIFO memory.

New written data shall occupy on the back of the last data as illustrated in Figure 3-4B. See section 3-4 for detail of the function of FIFO memory.

See section 3-2-4 for whole programming of the Paced Update operation.

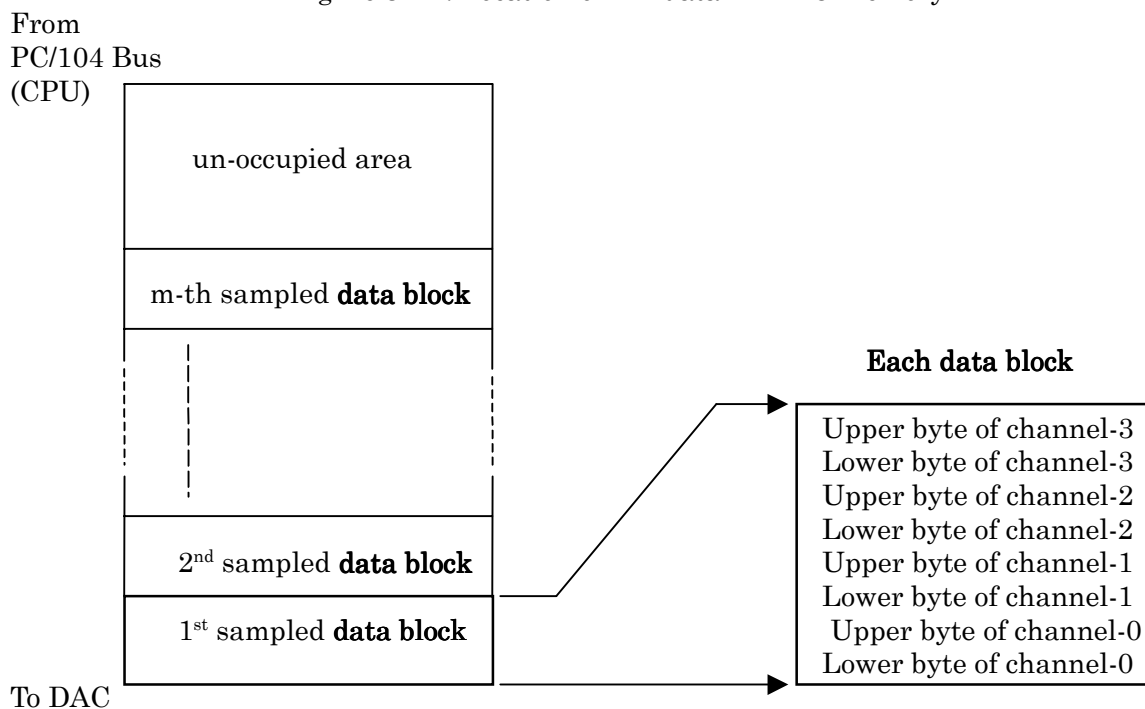
For example,

for  
one  
Update →

```
Outp (BASE+0x0, ch0-L) ; /* Lower byte data for Channel-0 */
Outp (BASE+0x0, ch0-U) ; /* Upper byte data for Channel-0 */
Outp (BASE+0x0, ch1-L) ; /* Lower byte data for Channel-1 */
Outp (BASE+0x0, ch1-U) ; /* Upper byte data for Channel-1 */
Outp (BASE+0x0, ch2-L) ; /* Lower byte data for Channel-2 */
Outp (BASE+0x0, ch2-U) ; /* Upper byte data for Channel-2 */
Outp (BASE+0x0, ch3-L) ; /* Lower byte data for Channel-3 */
Outp (BASE+0x0, ch3-U) ; /* Upper byte data for Channel-3 */
```

/\* Write sequential data into FIFO memory same as above \*/

Figure 3-4B. Location of DA-data in FIFO memory



### 3-16. Master-Slave Operation

Synchronized Master-Slave operation is also available with multiple boards.

Master-board provides the Pacer Clock to the Slave-boards for synchronizing the update between them.

#### On-Board Hardware Configurations.

- (1) Set those Address by the switches SW1, SW2, and SW3 with differences against each other. See section 3-5 for details.
- (2) Analog Output Range is on your choice, any differences between them do not cause trouble.
- (3) Set interrupt level by the jumper JP-INT of Master-board if use. See section 3-13 for details.
- (4) Set switch "S-CKZ" to "ON" at only one of the Slave board and set to "NC" for the others including Master board. This is the termination for the Clock Signal.

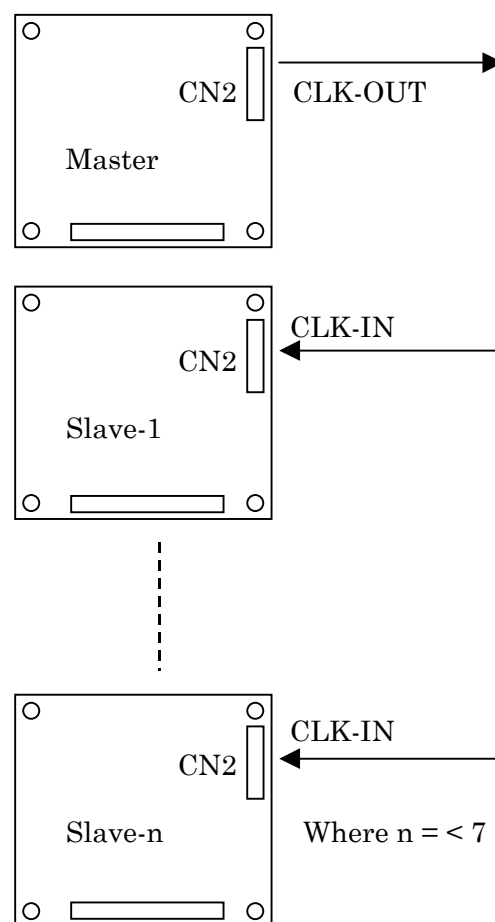
#### Board to Board Connections.

- (1) Pacer Clock Output (CLK-OUT) of Master must be connected to the External Clock Source Input (CLK-IN) of Slaves. Master can drive 7 Slaves directly. If more than 7 Slaves are needed, you can connect the Clock from 7<sup>th</sup> Slave to additional 7 Slaves as well as between Master and Slaves. See figure 3-16.
- (2) External Clock Source Input (CLK-IN) which can be divided and or External Trigger Input (TRG-IN) are available only to the Master.

#### Software Flow.

- (1) Select External Clock Source, and set divide ratio to "1/1" for all slaves. They must accept the Clock Source from the Master.
- (2) Write DA-data into each FIFO memory within the capacity.
- (3) Set Software Trigger and Start Command to all Slaves individually as waiting for the Pacer Clock from the Master before enable any Trigger and put Start Command to the Master.
- (4) Paced Operation shall be start by the Trigger to the Master.
- (5) Write DA-data into each FIFO memory by Polled Status or Interrupt Service. See <Note for Programming> in previous section 3-15 for details.

Figure 3-16. Master-Slave Connection



## 3-17. General Purpose Digital I/O

Din = inp (BASE+0xE) ; /\* Digital Inputs \*/  
 outp (BASE+0xE, GPQ) ; /\* General Purpose Digital Output \*/

**Digital Input**

Read (BASE+EH) Register specifies the 3bits current state external (74HCT-type CMOS) Inputs “CLK-IN”, “TRG-IN”, and “INT-IN” which assigned on Connector “CN2”.

See Figure 1-7 of section 1-7.

3 External Inputs should work for their own function with the program.

If they have not programmed for the function, they work for General Purpose (74HCT-type CMOS) Digital Input.

Table 3-17A. Read (BASE+EH) Register Bit Field.

Bit	Input assignment	“=1” specifies	“=0” specifies
B7 B6 B5 B4 B3	Not used		
B2	“CLK-IN” as External Clock Source Input	High (or Open)	Low
B1	“TRG-IN” as External Digital Trigger Input	High (or Open)	Low
B0	“INT-IN” as External Interrupt Input	High (or Open)	Low

**Digital Output**

Write (BASE+EH) Register specifies the 1bit of General Purpose Digital Output which

assigned on Connector “CN2”.

See Figure 1-7 of section 1-7.

Table 3-17B. Write (BASE+EH) Register Bit Field. / Where S-POL set to “N” /

Bit	Output assignment	“=1” specifies	“=0” specifies	On Reset
B7 B6 B5 B4 B3 B2 B1	Not used			0 0 0 0 0 0 0
B0	“GPQ-OUT” as General Purpose Digital Output	Low	High	0

## &lt;Note&gt;

Write (BASE+EH) Register is not cleared by Read (BASE+FH) Register as a Board-Reset Command, but cleared by the hardware reset or power-on process.

## &lt;Caution&gt;

Logical Polarity is set to Negative with setting the switch S-POL to “N” on shipping cause “GPQ-OUT” to CMOS high state at the hardware reset or power-on process. Typical 100ms width high state shall be appear on “GPQ-OUT” at the hardware reset or power-on process before set to Low state on Positive Logic with setting the switch S-POL to “P”

This is a character of the circuit.

## Section 4. Maintenance and Appendix

### 4-1. Trouble Shootings

#### **Reconfirm.**

The MDA-714PC104 supplied by MICRO SCIENCE is fully calibrated and tested. If it doesn't work on your system, reconfirm following issues.

- (1) Check the I/O BASE address specified by the on-board switch SW1, SW2, and SW3. On the IBM PC/AT compatible system, the I/O address must be mapped between "0H" to "3FFH" or the image of this range except for the occupied address by the other devices or the peripherals.
- (2) Debug your software or applications. For example, if the Interrupt level is correct or if occupied by any other devices. Are the Triggers suitable to the application? When the program is waiting for the Triggers, it seems that the program is stacked.
- (3) Be careful to input the signal at the Input of the External Digital Trigger "TRG-IN", Pacer Clock Source "CLK-IN", and Interrupt "INT-IN". Applying the voltage of higher than +7v or lower than -0.5v to these HCT-type CMOS inputs shall cause permanent destruction of the front-ended devices. For example, Multi Wave Form Generator is that!

#### **What's wrong?**

Fill in and send (Letter, Fax, or Email) the Q&A form to MICRO SCIENCE where you didn't find anything wrong. Although we will study about your system and answer by the letter what you should do, we don't write or debug application software. Sorry, we won't answer with any language but Japanese on the phone. Please write us Japanese or English.

#### **Replace the Board or Repair for free.**

MICRO SCIENCE will replace or repair the Board for free which are after examination disclosed to the satisfaction of MICRO SCIENCE to be thus defective, for a period within one year of shipment. This warranty shall not apply which have been subject to misuse, negligence, or accident. See "Caution/Warranty" for details in page-4.

#### **Repair the Board.**

MICRO SCIENCE will repair, calibrate, or test the Board on request. These products should have to prepaid the transportation at MICRO SCIENCE. Be sure, give us the information with the products, maybe Q&A form is useful for the report. Then user have to pay the proper cost in few weeks according to the bill after accept the returned products.

## 4-2. Calibration

MDA-714PC104 is supplied by MICRO SCIENCE fully calibrated and tested. However, before execute the user application and or at the chance of inspection for the system maintenance, you had better to calibrate the Board with the standard source.

### Procedure.

- (1) Measure the voltage between “TP+” and “TPG” as the test point of reference output.
- (2) Trim the POT “TM0” to have +10.000 v sharp, and your MDA-714PC104 is calibrated within 0.058% of Full-Scale plus accuracy of the volt meter.

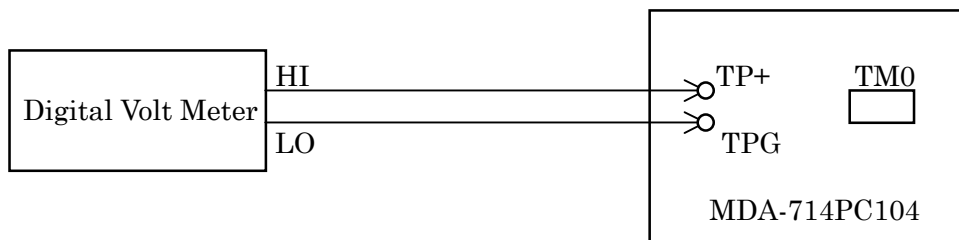
### <Note-1>

This adjustment is only for the reference voltage of MDA-714PC104. You have no way that Offset and Gain trimming for individual analog output. The optimizing adjustment for particular channel cause decrease the accuracy of other channels.

### <Note-2>

MDA-714PC104 is calibrated within 0.07% of Full-Scale accuracy at the factory of MICRO SCIENCE, though MDA-714PC104 has 0.004% of Full-Scale non-linearity, and 0.058% of Full-Scale differential accuracy among whole channels.

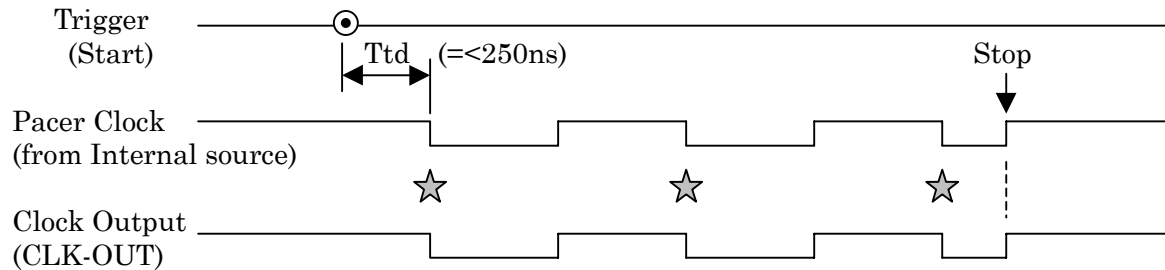
Figure 4-2. Measure between “TP+” and “TPG”





## 4-3. Trigger and Clock Timing for externals

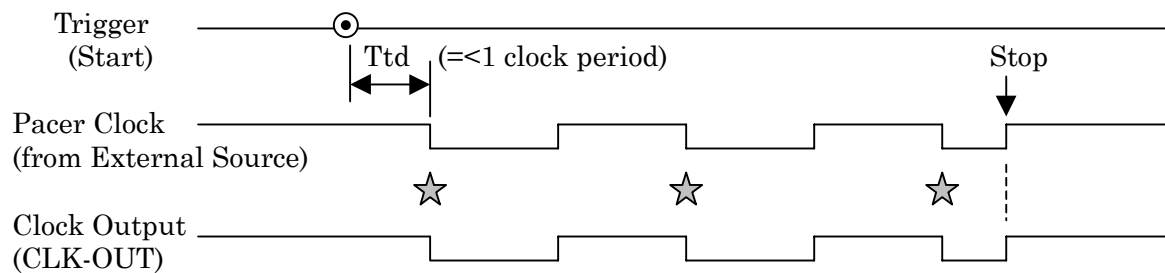
Figure 4-3A. Clock Output with Internal Clock Source



Where Ttd is the delay from the Trigger to the 1<sup>st</sup> Pacer Clock.

Valid edge of Pacer Clock and Clock Output is falling. → ☆

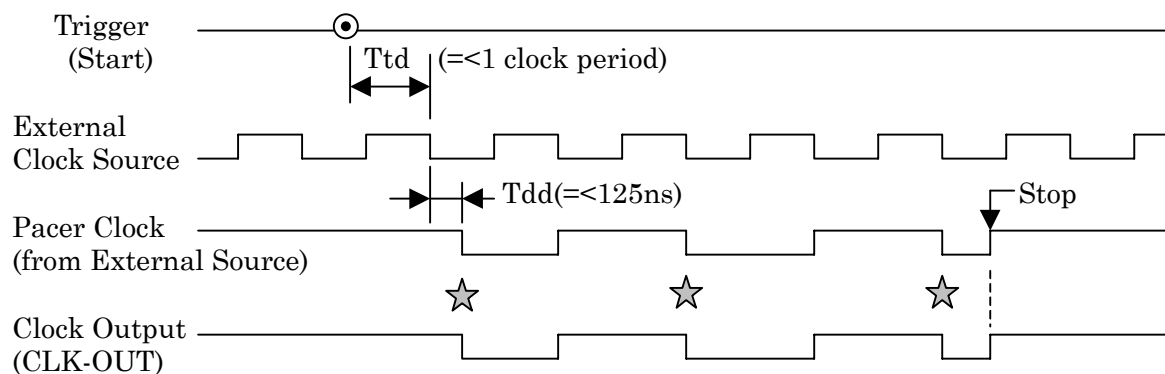
Figure 4-3B. Clock Output with External Clock Source (non-divided)



Where Ttd is the delay from the Trigger to the 1<sup>st</sup> Pacer Clock.

Valid edge of Pacer Clock and Clock Output is falling. → ☆

Figure 4-3C. Clock Output with External Clock Source (divided by 2)



Where Ttd is the delay from the Trigger to the 1<sup>st</sup> valid External Clock Source.

Tdd is the delay of the start to divide for Pacer Clock generation.

Valid edge of Pacer Clock and Clock Output is falling. → ☆

## Q & A form (in English or Japanese)

To:  
 MICRO SCIENCE., Co. LTD  
 Customer Support Div  
 2-37-12, Nishiogi-kita,  
 Suginami-ku,  
 Tokyo, Japan

From:

Fax: +81-3-3301-5593  
 Email: [gas@microscience.co.jp](mailto:gas@microscience.co.jp)

Fax:  
 Email:

<b>MDA-714PC104</b>	serial # =	Purchase Date:
Preferences on- Board	SW1 =	JP-INT =
	SW2 =	S-POL =
	SW3 =	S-CKO = , S-CKZ=
Other Devices In the system	Product:	
	Occupied Resources: (I/O Address = ), (Interrupt = )	
System Information	CPU:	
	OS :	
Software	Language:	
	Compiler:	

(Information)

<Note> MICR SCIENCE does not answer on phone with any language but Japanese.