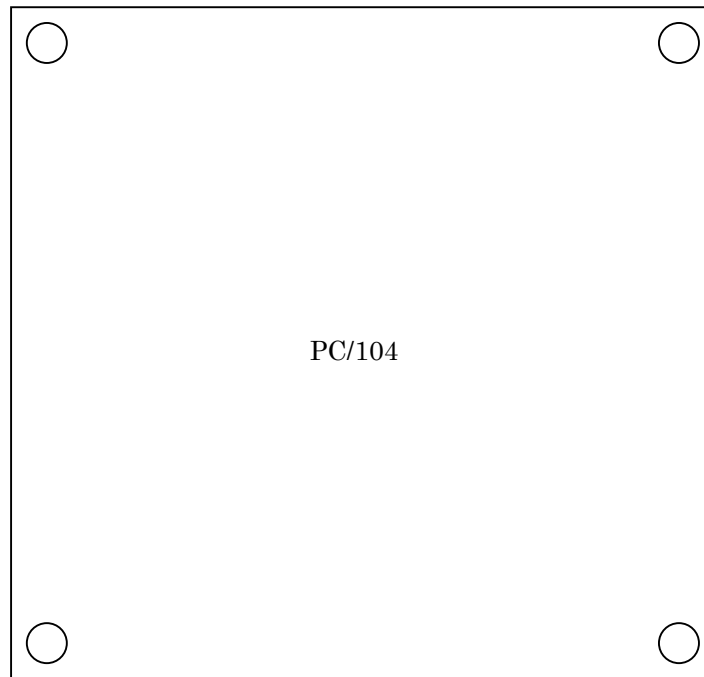


Real Solution for FA & LA



32-bit TTL Output, and 8-bit TTL Input

DIO-215PC104

User's Manual

for PC/104-BUS

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Caution

Unpacking

This package contain a DIO-215PC104 board, and 4 pieces of standoff.

Upon receipt the package, visually inspect the board for missing or damaged materials. This product was shipped in perfect condition as it was new.

Examine the package for physical damage. In the event of damage, save all packing materials and notify your courier to validate shipping claims.

Anti-static discharge

The DIO-215PC104 contains components that are susceptible to static discharge, and should be handled with appropriate caution. The anti-static packing material protects components from being damaged by static discharge.

Should the DIO-215PC104 board need to be returned for repair at a later date, it can be safely done by packing it in the original materials.

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Any said of products, at MICRO SCIENCE's factory or facility, should have to be prepaid transportation charges, and which are after examination disclosed to the satisfaction of MICRO SCIENCE to be thus defective, for a period within one year shipment.

These provisions do not extend the original warranty period of any product which has either been repaired or replaced by MICRO SCIENCE.

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In this Agreement, a "FILE" shall mean a contiguous collection of machine-readable symbols, bytes, characters, or codes which may be used by the CPU on the user's computer or processing equipment.

A "PROGRAM" is a file or related group of files which may be loaded and processed on the user's computer or processing equipment to perform the functions.

A "SOFTWARE" shall mean one or more FILES or PROGRAMS.

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MICRO SCIENCE will answer the written questions (including FAX, or Email) in Japanese or English from the registered user about this product.
Send us the question form in this manual filled with the information.

We do not answer on phone with any language but Japanese.
Although MICRO SCIENCE may offer advice, we will not design the user's application.

Price List (# on Jul, 2002)

Items	Unit Price	Description
DIO-215PC104	\$ 160.00	32-bit TTL Output and 8-bit Input board for PC/104
User's Manual	\$10.00	Printed one. (PDF file is free for download from the WEB)

The product consists of a DIO-215PC104 board and 4 pieces of standoff.

WEB : www.microscience.co.jp/eng/

Section 1. Introduction

1-1. Guide this Manual

This Manual contains a complete set of hardware and programming information for the DIO-215PC104 board, including configuration, installation, and I/O connection.

Section 1 contains the outline of functional descriptions and detail specifications, the installation, and setup procedure for the board.

Section 2 contains the digital input, output, and their timing information.

Section 3 contains the trouble-shootings, and repair.

The last page is the request form for the Q and A.

1-2. Functional Specification

Digital Inputs and Outputs.

Number of Output	32-bits (:8-bits x 4 ports) and the strobes for acceptors.
Output Level	TTL level, latched. (74LS04N assembled in the dual-in-line socket.)
Number of Input	8-bits and the strobe input.
Input Level	TTL level.

System Configuration

###: on-board switch programmable.

Bus Compatibility	PC/104 Bus, Data-bus is driven by 74HCT245, and all other signals are driven or accepted by (HCT-type) C-MOS devices.
Board Address ###	Upper 12Bits: programmable by on-board switches. Lower 4Bits: on-board logic decoded for multiple I/O ports.
Interrupt ###	IRQ3,4,5,6,7,9

I/O Connectors

for Digital Output	40pin FRC type (2.54mm pitch)
for Digital Input	20pin FRC type (2.54mm pitch)

Physical, Environmental

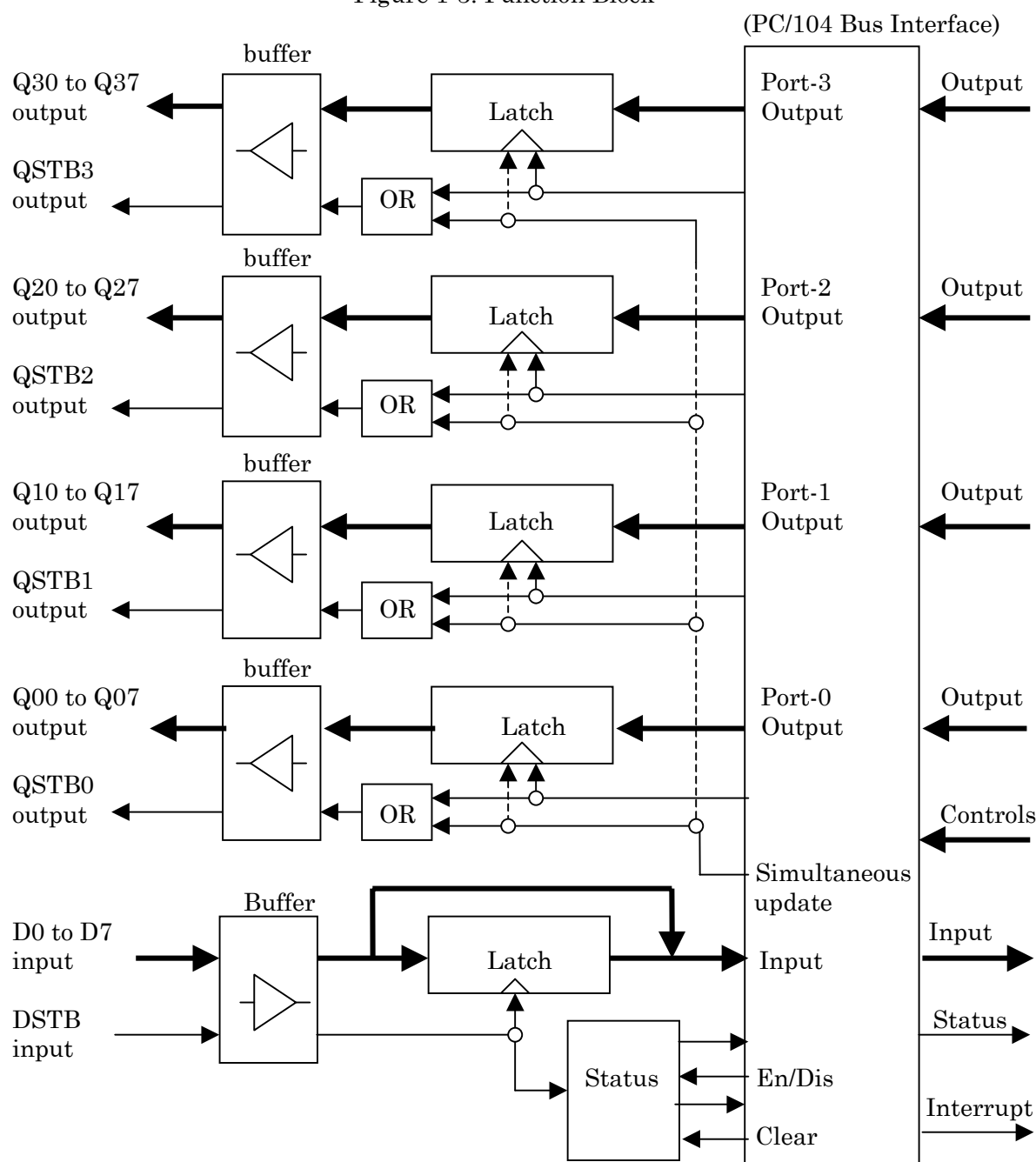
Operating Temperature Range	0 to +55
Storage Temperature Range	-10 to +85
Relative Humidity	80% (Non-condensing)
Power Supply, Consumption	+5v 0.33 A

1-3. Functional Description

DIO-215PC104 is designed for multiple digital input and output channels. General purpose 32-bit TTL outputs are consist of 8-bits by 4-ports, and the strobe output for each port are also available for the acceptors. These output elements are 74LS04 assembled in the socket.

It is also available for open collector output with replace the 74LS04 to 74LS06. General purpose 8-bit TTL inputs and the strobe input are available, too. You can read the current state of the input, or the state of last latched timing. The base address of the board is programmable with the on-board switches.

Figure 1-3. Function Block

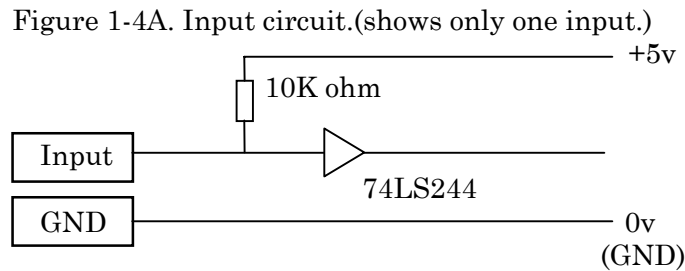


1-4. Input and Output circuit

Input.

All Inputs are TTL level, and pulled-up with 10K ohm resistor. See section 2-8 for programming.

Figure 1-4A shows the circuit.

**Output.**

All Outputs are also TTL level, latched, and you can select the logical polarity by on-board switch "S-POL".

MICRO SCIENCE set "S-POL" to "N" as negative logic, that cause all outputs to "TTL-High" level at the hardware reset in power-on process.

Figure 1-4B shows the circuit for all outputs and strobe outputs.

<Note-1>

All outputs are not cleared by the software reset with Read(BASE+7H) command but cleared by the hardware reset.

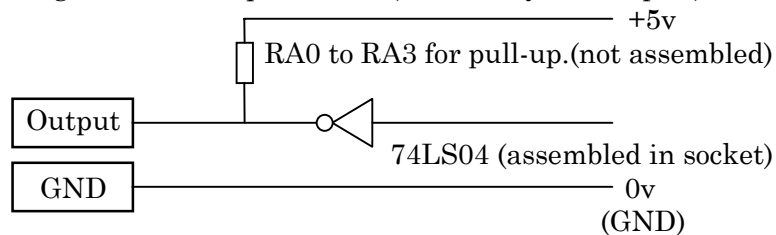
<Note-2>

74LS04 are assembled in the socket as TTL level digital output devices at the factory of MICRO SCIENCE.

You can replace them by 74LS06 or 74LS07 for change to open-collector level.

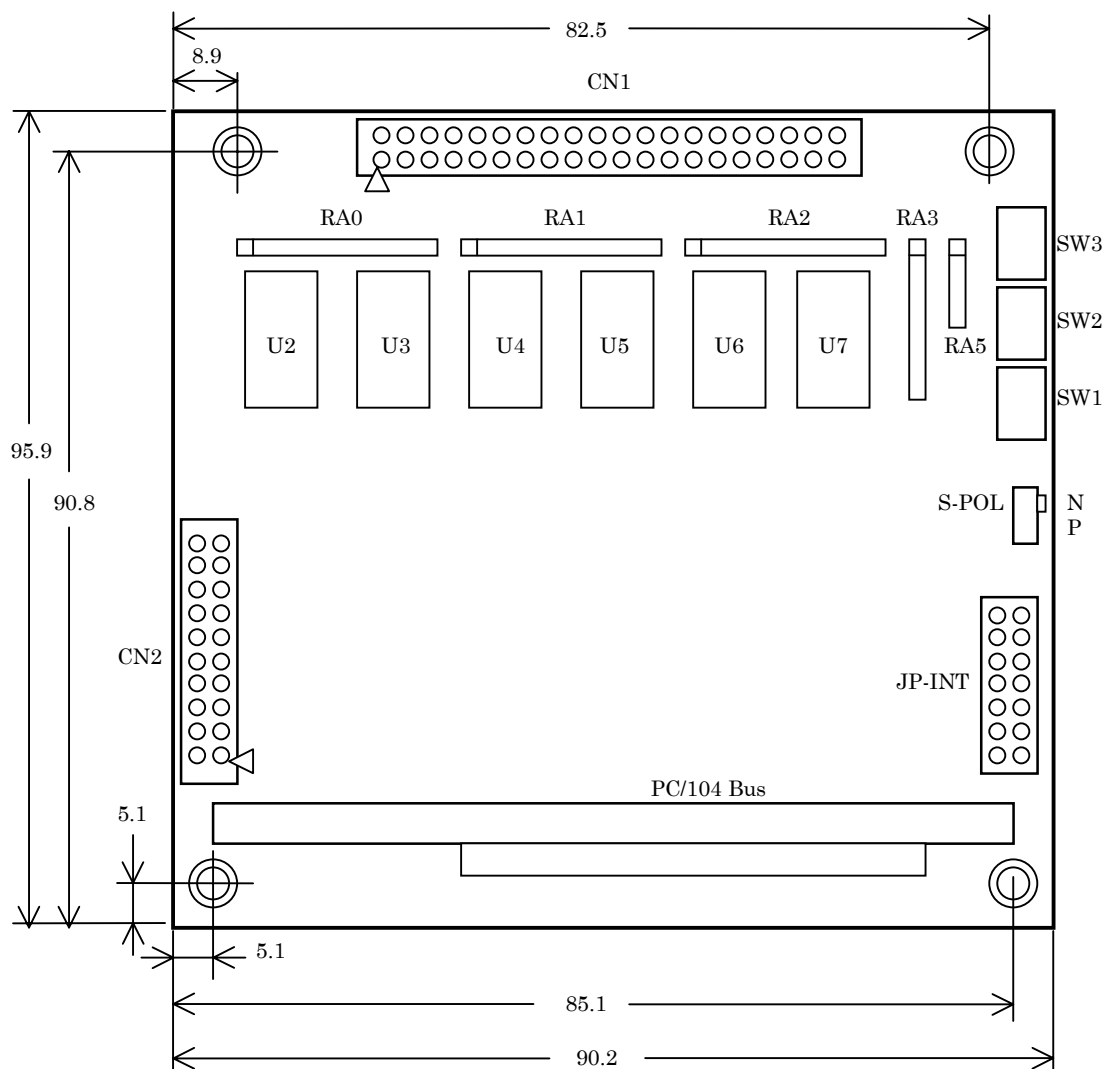
See section 2-9 for programming.

Figure 1-4B. Output circuit.(shows only one output.)



1-5. Layout of the board

Figure 1-5.



Unit: mm

At shipping, on-board programmable elements are set to < > position.

SW1, SW2, SW3 : Program switch for Base Address of the board. <0,1,C> / see 1-6-1./

JP-INT : Select jumper-switch for Interrupt Level. <NC> / see 1-6-2./

S-POL : Select switch for Logic Polarity of the Outputs. <N> / see 1-6-3 /

RA0 to RA3 : Pull-up resistor for Q00 to Q37 output. <Not assembled> / see 1-4 /

RA5 : Pull-up resistor for QSTB0 to QSTB3 output. <Not assembled> / see 1-4 /

U2 to U7 : Output device in the socket. <74LS04> / see 1-4 /

CN1 : Connector for Output (40pin FRC) / see 1-8 /

CN2 : Connector for Input (20pin FRC) / see 1-7 /

1-6. Settings on the board

1-6-1. BASE ADDRESS

DIO-215PC104 appears as a 16-byte block of registers within the host CPU's I/O address space. This address block must not conflict with other system I/O devices.

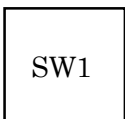

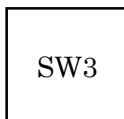
You can program the on-board switches SW1, SW2, and SW3 as BASE ADDRESS of the board.

These hex-a-decimal defined switches are set to SW1=0, SW2=1, SW3=C at the factory of MICRO SCIENCE, that define the BASE ADDRESS to "01C0" hex.

DIO-215PC104 occupies upper 16 byte address from the BASE.

See section 2-2 for more information.








Figure 1-6A. Setting the BASE ADDRESS

Address Line →	AB15 to AB12	AB11 to AB08	AB07 to AB04	AB03 to AB00
On-board Hex-a-decimal → Switches				on-board logic decoded for multiple ports
Factory setting →	0	1	C	(F to 0)

1-6-2. Interrupt Level

Strobe inputs "DSTB" can cause an interrupt request to the CPU. Select the interrupt level by the jumper-switch "JP-INT", and program Write (BASE+7H) register to enable the state. See section 2-5 for the details.

Figure 1-6B. select the Interrupt Level.

JP-INT	(Level)
	IRQ3
	IRQ4
	IRQ5
	IRQ6
	IRQ7
	IRQ9
	NC (non-connected)

1-6-3. Output Logic Polarity

DIO-215PC104 has 32-bits TTL level output for general purpose.

Select the logical polarity of the outputs by the switch "S-POL".

This switch is set to "N" at the factory of MICRO SCIENCE that defines the logical polarity to "Negative".

You can also set to "P" for "Positive".

See section 2-9 for the programming.

1-7. Digital Input Connector

8-bits Parallel Digital Inputs are available on 20-pin FRC-type male connector CN2 on the board as illustrated in Figure 1-5.

The plug is also provided for general purpose, come with the board.
See section 2-8 for programming.

Figure 1-7. Digital Input Connector CN2 pin assignment

Function	Sign	Pin assign		Sign	Function
Digital Input D0	D0	1	O O	2	GND
D1	D1	3	O O	4	GND
D2	D2	5	O O	6	GND
D3	D3	7	O O	8	GND
D4	D4	9	O O	10	GND
D5	D5	11	O O	12	GND
D6	D6	13	O O	14	GND
D7	D7	15	O O	16	GND
Input strobe	DSTB	17	O O	18	GND
+5v Output	+5v	19	O O	20	GND

<Note-1> On-board bracket : Model= HIF3FC-20PA-2.54DSA /made by HIROSE/
Plug : Model= HIF3BA-20DA-2.54R(11) /made by HIROSE/

<Note-2> +5v Output is supplied from PC/104 Bus.

1-8. Digital Output Connector

Digital Outputs are available on a 40-pin FRC-type male connector CN1 on the board as illustrated in Figure 1-5. All outputs have the capability for 10 TTL load.

See section 2-9 for programming.

The plug is also provided for general purpose, come with the board.

Figure 1-8. Digital Output Connector CN1 pin assignment

Function	Sign	Pin assign		Sign	Function
(Port-0) Output 00	Q00	1	O O	2	Q01 (Port-0) Output 01
02	Q02	3	O O	4	Q03 03
04	Q04	5	O O	6	Q05 05
06	Q06	7	O O	8	Q07 07
(Port-1) Output 10	Q10	9	O O	10	Q11 (Port-1) Output 11
12	Q12	11	O O	12	Q13 13
14	Q14	13	O O	14	Q15 15
16	Q16	15	O O	16	Q17 17
(Port-2) Output 20	Q20	17	O O	18	Q21 (Port-2) Output 21
22	Q22	19	O O	20	Q23 23
24	Q24	21	O O	22	Q25 25
26	Q26	23	O O	24	Q27 27
(Port-3) Output 30	Q30	25	O O	26	Q31 (Port-3) Output 31
32	Q32	27	O O	28	Q33 33
34	Q34	29	O O	30	Q35 35
36	Q36	31	O O	32	Q37 37
Ground	GND	33	O O	34	GND Ground
Output strobe for Port-0	QSTB0	35	O O	36	QSTB1 Output strobe for Port-1
Output strobe for Port-2	QSTB2	37	O O	38	QSTB3 Output strobe for Port-3
Ground	GND	39	O O	40	GND Ground

<Note> On-board bracket : Model=HIF3FC-40PA-2.54DSA /made by HIROSE/
 Plug : Model=HIF3BA-40DA-2.54R(11) /made by HIROSE/

Section 2. General Programming

2-1. General Programming Information

Handling

DIO-215PC104 appears to the host PC/104 bus CPU as a block of contiguous 16 hardware registers mapped within the I/O address space. See Table.2-2 for the map. These registers control the operation of DIO-215PC104 as long as they are accessed using 16bit I/O addressing with each 8bit data transfers.

These registers include Reset-board, General Purpose Digital I/O, Interrupt, and Status.

Operation

Entire information for programming are specified and explained in order as follows.

(section 2-1)

General software sequences for reading input, writing output, and Interrupt control.

(section 2-2 to 2-9)

The functions of each register. These are the elements for programming.

----- Typical software sequence -----

(1)

Set input strobe condition.

Outp (BASE+0x5, DSTB) ; /* Enable/Disable, and Polarity */

(2)

Read input.

CD0 = inp (BASE+0x0) ; /* Read current input D0 to D7 */

LD0 = inp (BASE+0x8) ; /* Read latched input D0 to D7 */

(3)

Write output.

Outp (BASE+0x6, upm) ; /* Update mode */
; /* Individually, or Simultaneously */

Outp (BASE+0x0, P0Q) ; /* Output Q00 to Q07, Latched */

Outp (BASE+0x1, P1Q) ; /* Output Q10 to Q17, Latched */

Outp (BASE+0x2, P2Q) ; /* Output Q20 to Q27, Latched */

Outp (BASE+0x3, P3Q) ; /* Output Q30 to Q37, Latched */

UPD = inp (BASE+0x6) ; /* Simultaneous update all */

(4)

Set interrupt condition.

Outp (BASE+0x7, icc) ; /* specify the interrupt conditions */

(5)

Polling for detecting the strobe.

While ((inp(BASE+0x4) & 0xFF) == 0x00) ; /* Detecting the strobe */

2-2. I/O Register Map

DIO-215PC104 appears as a 16-byte block of registers within the host CPU's I/O address space. This address block must not conflict with other system I/O devices.

You can program the on-board switches SW1, SW2, and SW3 as BASE ADDRESS of the board.

These hex-a-decimal defined switches are set to SW1=0, SW2=1, SW3=C at the factory of MICRO SCIENCE, that specify the BASE ADDRESS to "01C0" hex.

DIO-215PC104 occupies upper 16 byte address from the BASE.

See figure 1-5 for the location of the board.

Figure 1-6A. Setting the BASE ADDRESS

Address Line →	AB15 to AB12	AB11 to AB08	AB07 to AB04	AB03 to AB00
On-board Hex-a-decimal Switches →	SW1	SW2	SW3	on-board logic decoded for multiple ports
Factory setting →	0	1	C	(F to 0)

Table 2-2. DIO-215PC104 Register Assignment. (All the port consist of 8bit.)

I/O Address	Direction	Description	Refer to
BASE +8H	Read	Latched input D0 to D7 (Port-0)	Section 2-8
	Write		
BASE +7H	Read	Reset Board, and get ID.	Section 2-3
	Write	Interrupt control. (Enable/Disable, Polarity)	Section 2-5
BASE +6H	Read	Simultaneous update operation.	Section 2-9
	Write	Update mode selection.	Section 2-6
BASE +5H	Read		
	Write	Input strobe control. (Enable/Disable, Polarity)	Section 2-4
BASE +4H	Read	Get status.	Section 2-7
	Write	Clear status.	
BASE +3H	Read		
	Write	Update output Q30 to Q37 (Port-3, Latched)	Section 2-9
BASE +2H	Read		
	Write	Update output Q20 to Q27 (Port-2, Latched)	Section 2-9
BASE +1H	Read		
	Write	Update output Q10 to Q17 (Port-1, Latched)	Section 2-9
BASE +0H	Read	Current input D0 to D7 (Port-0)	Section 2-8
	Write	Update output Q00 to Q07 (Port-0, Latched)	Section 2-9

	Not-used
--	----------

2-3. Reset the Board, and get ID

```
rst = inp (BASE+0x7) ; /* Reset the Board */
```

Read (BASE+7H) Register cause the board reset.
All registers of the board must be initialized except for the last values of General Purpose Digital Output described in section 2-9.

Where “rst” is the ID that depend on the board, “26H” for DIO-215PC104.

Table 2-3. Read (BASE+7H) Register Bit Field.

Bit	Description
B7	26H is the ID for DIO-215PC104.
B6	
B5	
B4	
B3	
B2	
B1	
B0	

2-4. Input Strobe Control

```
outp (BASE+0x5, SIC) ; /* Specify the Input Strobe */
```

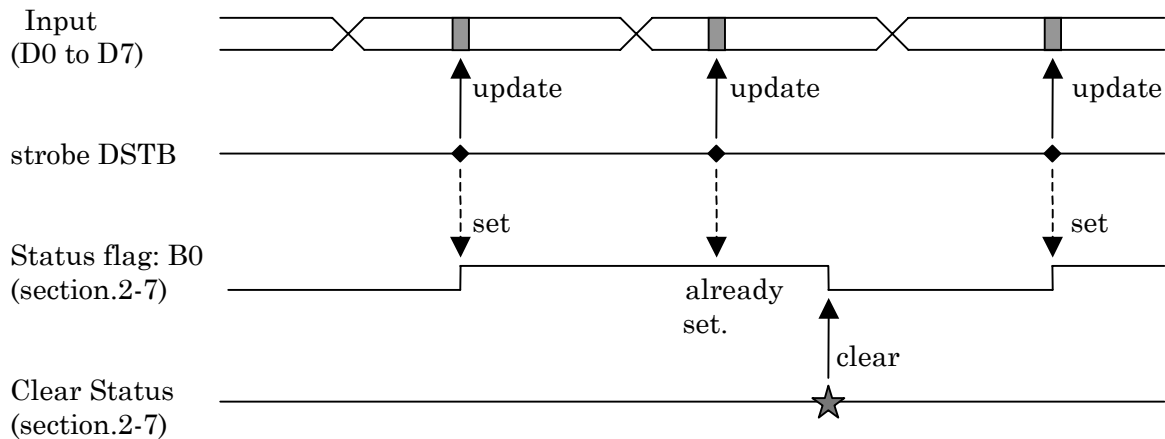
Write (BASE+5H) Register specifies the input strobe for control the latch.

Enabled strobe shall update the latch and set the appropriate flag of the status.
See Table.2-8B and Table 2-7A for the result.

Table 2-4. Write (BASE+5H) Register Bit Field.

Bit	Term	"=1" specifies	"=0" specifies	On reset
B7				0
B6				0
B5				0
B4	Valid Polarity of the strobe "DSTB"	Rising Edge	Falling Edge	0
B3				0
B2				0
B1				0
B0	Enable/Disable of the strobe "DSTB"	Enable	Disable	0

Figure 2-4. Latching operation by the strobe enabled.



Where, ♦ is the valid edge of the strobe input, ■ is the stored data.

2-5. Interrupt Control

```
outp (BASE+0x7, IC) ; /* Interrupt Control */
```

Write (BASE+7H) Register specifies the input strobe for control the interrupt request.

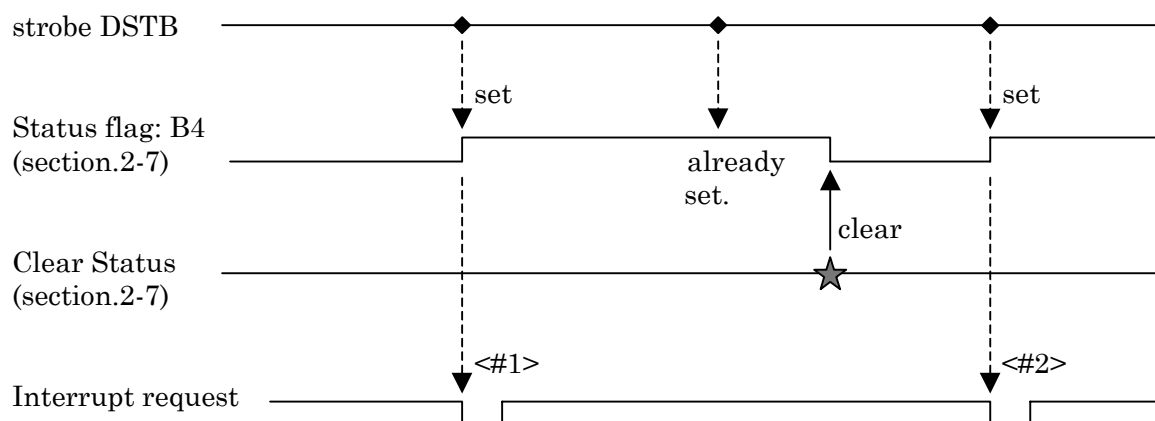
Enabled strobe shall cause generating the interrupt request and set the status flag. See Table 2-7A for the result. Interrupt request shall not be generated again before clear the status flag.

Table 2-5. Write (BASE+7H) Register Bit Field.

Bit	Term	"=1" specifies	"=0" specifies	On reset
B7				0
B6				0
B5				0
B4	Valid Polarity of the strobe "DSTB"	Rising Edge	Falling Edge	0
B3				0
B2				0
B1				0
B0	Enable/Disable of the strobe "DSTB"	Enable	Disable	0

(#) : Interrupt pulse to the PC/104 bus is 500ns width, and selected by "JP-INT" on the board illustrated in figure 1-5 & 1-6B.

Figure 2-5. Interrupt request by the enabled strobe.



Where, ◆ is the valid edge of the strobe input.

<#1> The first strobe generate the interrupt request.

<#2> Next interrupt request is generated as same as <#1> after clear status.

2-6. Output Update Mode

Outp (BASE+0x6, UPM) ; /* Output Update mode */

Write (BASE+6H) Register specifies the Output Update mode either Individual or Simultaneous

On the Individual mode, each output port shall be updated immediately by the output command.

On the Simultaneous mode, all output data shall be stored in the pre-latch buffer area by the output command, then updated simultaneously by Read (BASE+6H) command.

Table 2-6. Write (BASE+6H) Register Bit Field.

Bit	Term	"=1" specifies	"=0" specifies	On reset
B7				0
B6				0
B5				0
B4				0
B3				0
B2				0
B1				0
B0	Output Update mode selection	Simultaneous	Individual	0

2-7. Get Status and Clear Status

```
STS = inp (BASE+0x4) ; /* Get Status Flags */
```

Status data shall be read from (BASE+4H) Register.
Enabled input strobe set the flag as it accepted.

<Note>
Interrupt request shall not be generated again before clear the status flag.

Table 2-7A. Read (BASE+4H) Register Bit Field.

Bit	Term	"=1" specifies	"=0" specifies	On reset
B7				0
B6				0
B5				0
B4	Enabled strobe "DSTB" for interrupt	Accepted.	Not-Accepted.	0
B3				0
B2				0
B1				0
B0	Enabled strobe "DSTB" for latching	Accepted.	Not-Accepted.	0

```
outp (BASE+0x4, CLR) ; /* Clear Status Flags */
```

Write (BASE+0x4) Register command
makes clear the flags.

Table 2-7B. Write (BASE+4H) Register Bit Field.

Bit	Term	"=1" specifies	"=0" specifies	On reset
B7				0
B6				0
B5				0
B4	Enabled strobe "DSTB" for interrupt	Clear	Non-Effect	0
B3				0
B2				0
B1				0
B0	Enabled strobe "DSTB" for latching	Clear	Non-Effect	0

2-8. Read inputs

CD0 = inp (BASE+0x0) ; /* Read current input D0 to D7 */

Current state of inputs shall be read from (BASE+0H) Register.

See section 1-4 for the circuit, and section 1-7 for assignment of the connector.

Table 2-8A. Current input register bit field.

Bit	Term	"=1" specifies	"=0" specifies
B7	Current state of Input "D7"	TTL " High "	TTL " Low "
B6	Current state of Input "D6"		
B5	Current state of Input "D5"		
B4	Current state of Input "D4"		
B3	Current state of Input "D3"		
B2	Current state of Input "D2"		
B1	Current state of Input "D1"		
B0	Current state of Input "D0"		

Read Latched Input

LD0 = inp (BASE+0x8) ; /* Read latched input d0 to d7 */

Latched inputs shall be read from (BASE+8H) Register.

The data shall be updated by enabled strobe input and cleared by the software reset, or the power-on hardware reset .

Table 2-8B. Read (BASE+8H) Register Bit Field.

Bit	Term	"=1" specifies	"=0" specifies	on Reset
B7	Latched Input "d7"	TTL " High "	TTL " Low "	0
B6	Latched Input "d6"			0
B5	Latched Input "d5"			0
B4	Latched Input "d4"			0
B3	Latched Input "d3"			0
B2	Latched Input "d2"			0
B1	Latched Input "d1"			0
B0	Latched Input "d0"			0

2-9. Update Output

```

outp (BASE+0x6, UPM) ; /* Output Update mode, see section 2-6 */
outp (BASE+0x0, P0Q) ; /* Update Output Q00 to Q07 */
outp (BASE+0x1, P1Q) ; /* Update Output Q10 to Q17 */
outp (BASE+0x2, P2Q) ; /* Update Output Q20 to Q27 */
outp (BASE+0x3, P3Q) ; /* Update Output Q30 to Q37 */
UPD=inp(BASE+0x6) ; /* Simultaneous update, see section 2-6 */

```

Write (BASE+0H), (BASE+1H), (BASE+2H), (BASE+3H) register updates the output. They are TTL level (74LS04), and latched. See section 1-4 for the circuit, and section 1-8 for assignment of the connector.

Table 2-9. Output register bit field.

Bit	(BASE+0H)	(BASE+1H)	(BASE+2H)	(BASE+3H)	
B7	Output "Q07"	Output "Q17"	Output "Q27"	Output "Q37"	<Note-1> <Note-2> <Note-3>
B6	Output "Q06"	Output "Q16"	Output "Q26"	Output "Q36"	
B5	Output "Q05"	Output "Q15"	Output "Q25"	Output "Q35"	
B4	Output "Q04"	Output "Q14"	Output "Q24"	Output "Q34"	
B3	Output "Q03"	Output "Q13"	Output "Q23"	Output "Q33"	
B2	Output "Q02"	Output "Q12"	Output "Q22"	Output "Q32"	
B1	Output "Q01"	Output "Q11"	Output "Q21"	Output "Q31"	
B0	Output "Q00"	Output "Q10"	Output "Q20"	Output "Q30"	

<Note-1>

Logical Polarity is set to Negative with setting the switch S-POL to "N" on shipping cause all outputs to TTL high state at the hardware reset in the power-on process. See section 1-6-3 for settings.

<Note-3>

Open collector level is also available with replace the 74LS04 to 74LS06 in the socket. Strobe output "QSTB0,1,2,3" belongs to that.

<Note-2>

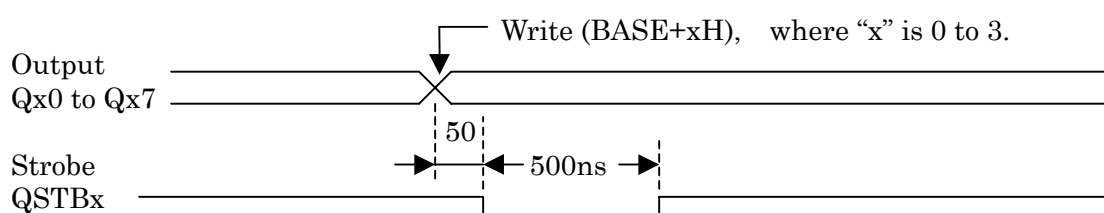
Latched outputs are not cleared by the software reset command, but cleared by the hardware reset in the power-on process.

Strobe Output

Typical 500ns width strobe pulse shall be appear on the "QSTBx" output at the writing (BASE+xH) register as an output update.

The Logical Polarity of strobe output is also specifies by the switch "S-POL", see section 1-6-3 for the settings.

Figure 2-9. "Qx0 to Qx7" and "QSTBx" output timing.



Section 3. Maintenance and Appendix

3-1. Trouble Shootings

Reconfirm.

The DIO-215PC104 supplied by MICRO SCIENCE is fully inspected and tested. If it doesn't work on your system, reconfirm following issues.

- (1) Check the I/O BASE address specified by the on-board switch SW1, SW2, and SW3. On the IBM PC/AT compatible system, the I/O address must be mapped between "0H" to "3FFH" or the image of this range except for the occupied address by the other devices or the peripherals.
- (2) Debug your software or applications. For example, if the Interrupt level is correct or if occupied by any other devices.
- (3) Be careful to connect the inputs, and outputs.

What's wrong?

Fill in and send (Letter, Fax, or Email) the Q&A form to MICRO SCIENCE where you didn't find anything wrong.

Although we will study about your system and answer by the letter what you should do, we don't write or debug application software.

Sorry, we won't answer with any language but Japanese on the phone.

Please write us Japanese or English.

Replace the Board or Repair for free.

MICRO SCIENCE will replace or repair the Board for free which are after examination disclosed to the satisfaction of MICRO SCIENCE to be thus defective, for a period within one year of shipment. This warranty shall not apply which have been subject to misuse, negligence, or accident. See "Caution/Warranty" for details in page-3.

Repair the Board.

MICRO SCIENCE will repair, calibrate, or test the Board on request. These products should have to prepaid the transportation at MICRO SCIENCE. Be sure, give us the information with the products, maybe Q&A form is useful for the report.

Then user have to pay the proper cost in few weeks according to the bill after accept the returned products.

Q & A form (in English or Japanese)

To:
 MICRO SCIENCE., Co. LTD
 Customer Support Div
 2-37-12, Nishiogi-kita,
 Suginami-ku,
 Tokyo, Japan

From:

Fax: +81-3-3301-5593
 Email: gas@microscience.co.jp

Fax:
 Email:

DIO-215PC104	serial # =	Purchase Date:
Preferences on- Board	SW1 =	JP-INT = 3, 4, 5, 6, 7, 9
	SW2 =	
	SW3 =	S-POL = N, P
Other Devices In the system	Product:	
	Occupied Resources: (I/O Address =), (Interrupt =)	
System Information	CPU:	
	OS :	
Software	Language:	
	Compiler:	

(Information)

<Note> MICR SCIENCE does not answer on phone with any language but Japanese.