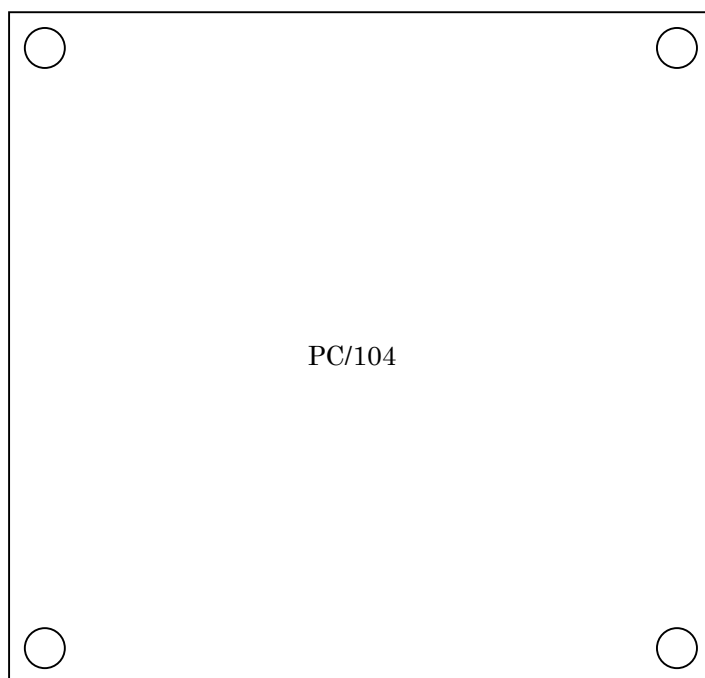


Real Solution for FA & LA



16-bit Isolation Digital Input with watching state,
and 4-bit non-isolation TTL output

DIO-216PC104

User's Manual

for PC/104-BUS

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Caution

Unpacking

This package contain a DIO-216PC104 board, and 4 pieces of 15mm standoff. Upon receipt the package, visually inspect the board for missing or damaged materials. This product was shipped in perfect condition as it was new.

Examine the package for physical damage. In the event of damage, save all packing materials and notify your courier to validate shipping claims.

Anti-static discharge

The DIO-216PC104 contains components that are susceptible to static discharge, and should be handled with appropriate caution. The anti-static packing material protects components from being damaged by static discharge.

Should the DIO-216PC104 board need to be returned for repair at a later date, it can be safely done by packing it in the original materials.

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These provisions do not extend the original warranty period of any product which has either been repaired or replaced by MICRO SCIENCE.

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A "PROGRAM" is a file or related group of files which may be loaded and processed on the user's computer or processing equipment to perform the functions.

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MICRO SCIENCE will answer the written questions (including FAX, or Email) in Japanese or English from the registered user about this product.
Send us the question form in this manual filled with the information.

We do not answer on phone with any language but Japanese.
Although MICRO SCIENCE may offer advice, we will not design the user's application.

Price List (# on Feb, 2002)

Items	Unit Price	Description
DIO-216PC104	\$ 190.00	16-bit Isolation Digital Input board for PC/104
User's Manual	\$10.00	Printed one. (PDF file is free for download from WEB)

The product consists of a DIO-216PC104 board and 4 pieces of standoff.

WEB : www.microscience.co.jp/eng/

Section 1. Introduction

1-1. Guide this Manual

This Manual contains a complete set of hardware and programming information for the DIO-216PC104 board, including configuration, installation, and I/O connection.

Section 1 contains the outline of functional descriptions and detail specifications, the installation, and setup procedure for the board.

Section 2 contains the digital input, output and watching the input state operation. Section 3 contains the trouble-shootings, and repair.

The last page is the request form for the Q and A.

1-2. Functional Specification

Digital Inputs and Outputs.

Number of Input	16-bits :(8-bits x 2 ports)
Input Level	Photo coupler isolated (typ)5mA current input, Requires external power supply : recommended 24v, also usable between 5v to 24v with additional resistor.
Input protection	125v DC(AC/peak) between each input and PC/104 bus. 50v DC(AC/peak) between the input and the other inputs.
Number of Output	4-bits.
Output Level	TTL level, latched. (74LS04N assembled in the dual-in-line socket.)

Watching Operation

Number of Input	16-bits :(8-bits x 2 ports) as same as above.
Detection of	The change state of any input.
Results	On detecting the change, set the flag, interrupt request (if enabled), and latch the all inputs into particular registers.

System Configuration

###: on-board switch programmable.

Bus Compatibility	PC/104 Bus All signals are driven or accepted by the C-MOS device. (74HCT type)
Board Address ###	Upper 12Bits: programmable by on-board switches. Lower 4Bits: on-board logic decoded for multiple I/O ports.
Interrupt ###	IRQ3,4,5,6,7,9

I/O Connectors

for Digital Input	40pin FRC type (2.54mm pitch)
for Digital Output	10pin FRC type (2.54mm pitch)

Physical, Environmental

Operating Temperature Range	0 to +55
Storage Temperature Range	-10 to +85
Relative Humidity	80% (Non-condensing)
Power Supply, Consumption	+5v 0.5 A

1-3. Functional Description

DIO-216PC104 is designed for multiple digital input channels with the photo-coupler isolation.

It is also available that watching function for detecting the change state of the specified inputs.

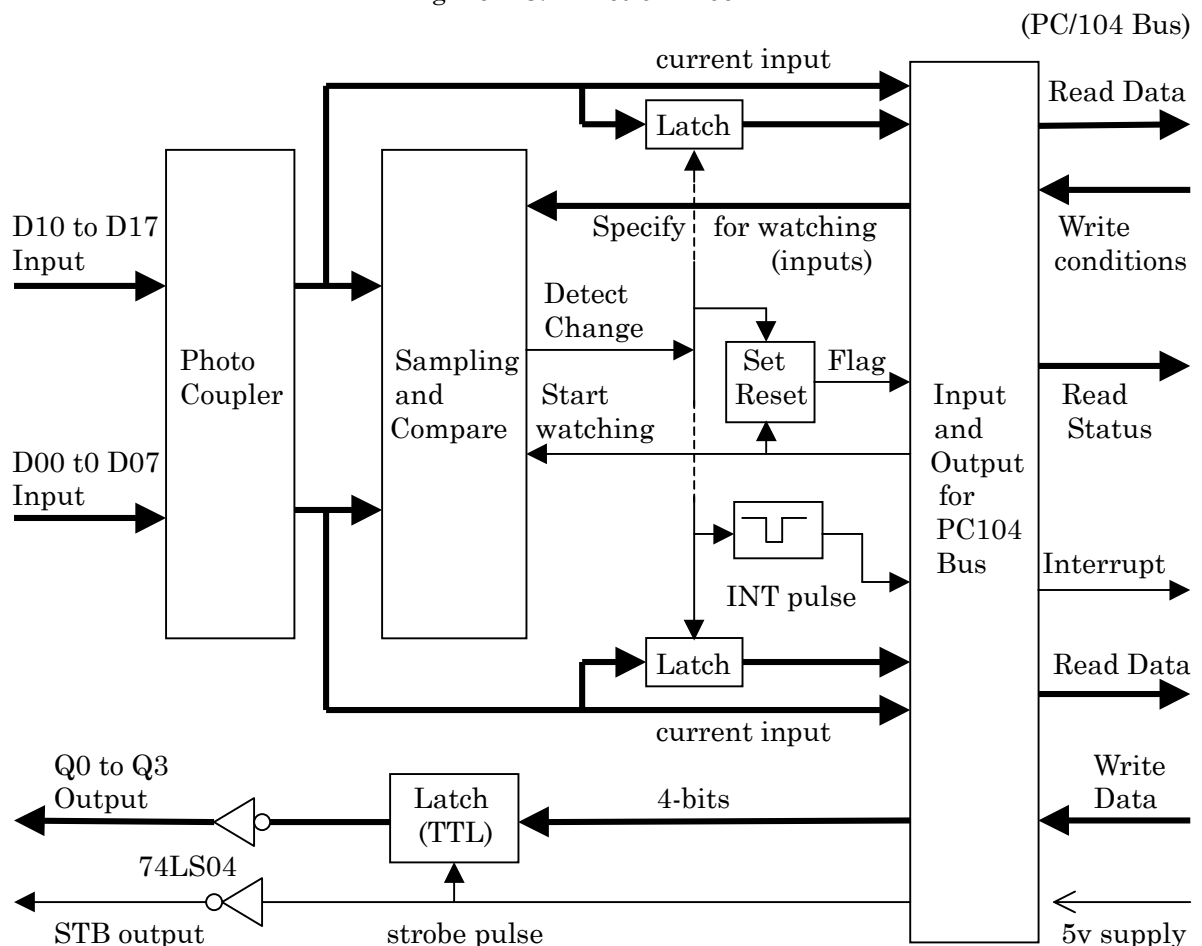
Detecting the change of any input of them cause set the flag and generate interrupt process if its enabled.

This function allows the system to have the fast response following the change state of inputs.

General purpose 4-bit TTL latched outputs and the update strobe pulse output are available with assembled 74LS04 in socket. It is also available for open collector output with replace the 74LS04 to 74LS06.

The base address of the board is programmable with the on-board switches.

Figure 1-3. Function Block



1-4. Input and Output circuit

Figure 1-4A shows the typical connection with the external circuits for the photo coupler isolated inputs.

It is required 24v external power supply, or 12v to 5v supply with the additional resistors as illustrated in Figure 1-4B.

Figure 1-4A. Typical Input circuit connection. (shows only one input.)

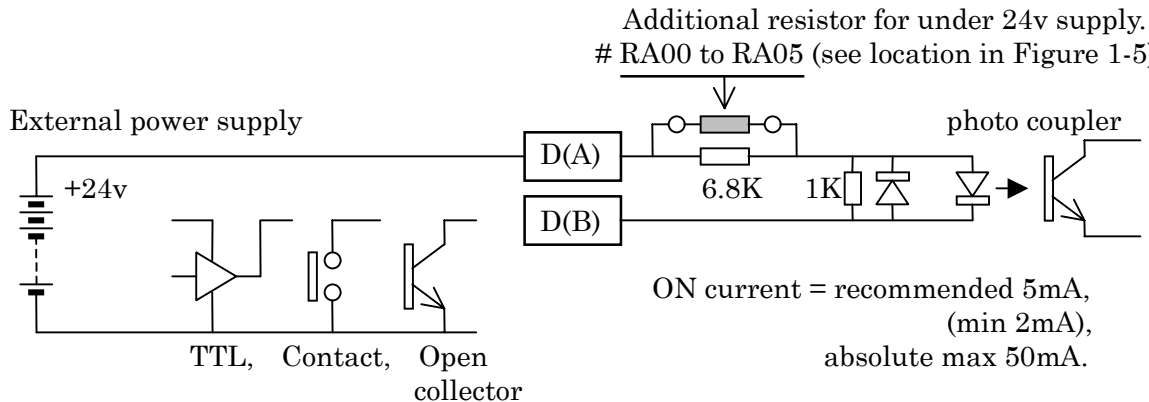
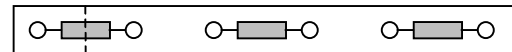


Figure 1-4B. Resistor array #RA00 to RA05

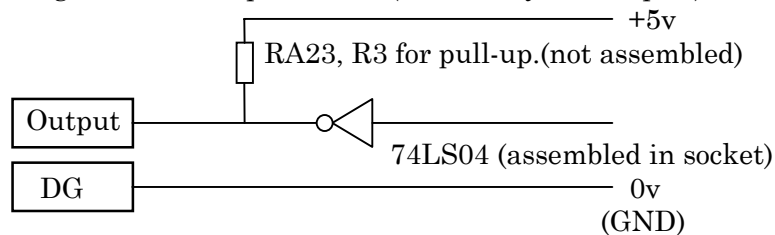


Where the value is 6.8K ohm for 12v supply, or 1.5K ohm for 5v supply.

Output.

Figure 1-4C shows the circuit for Q0 to Q3 and strobe "STB" output.

Figure 1-4C. Output circuit.(shows only one output.)



<Note-1>

Logical Polarity is set to Negative with setting the switch S-POL to "OFF" on shipping cause all outputs to TTL high state at the hardware reset in the power-on process.

Typical 100ms width high state shall be appear on all outputs at the hardware reset in the power-on process before set to Low state on Positive Logic with setting the switch S-POL to "ON".

This is a character of the circuit.

<Note-2>

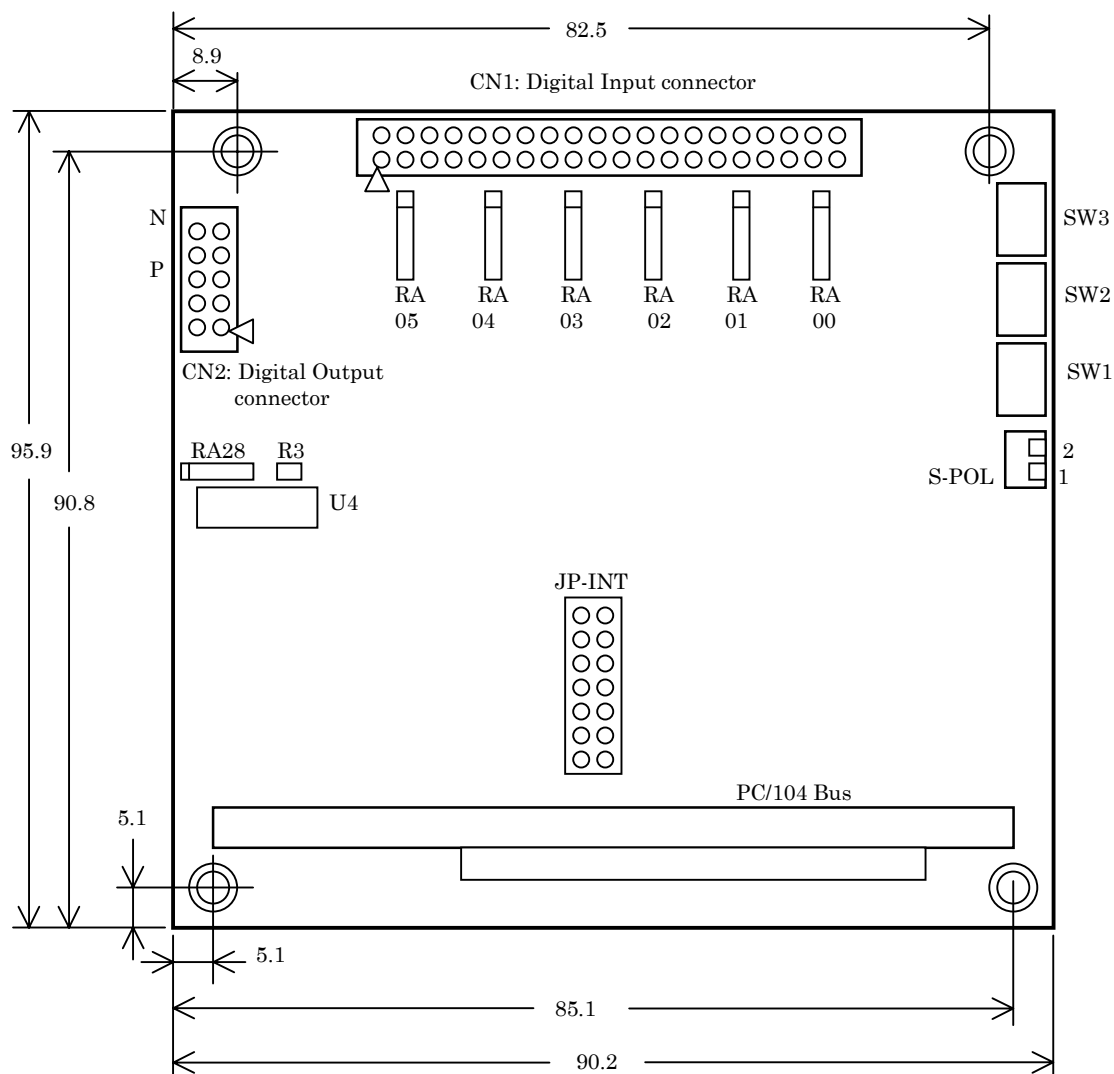
Latched output Q0 to Q3 are not cleared by the software reset command, but cleared by the hardware reset in the power-on process.

<Note-3>

Open collector level is also available with replace the 74LS04 to 74LS06 in the socket.

1-5. Layout of the board

Figure 1-5.



Unit: mm

At shipping, on-board programmable elements are set to < > position.

- # SW1, SW2, SW3: Program switch for Base Address of the board. <0,1,C> / see 1-6-1./
- # JP-INT: Select jumper-switch for Interrupt Level. <NC> / see 1-6-2./
- # S-POL: Select switch for Logic Polarity of the Outputs. <OFF> / see 1-6-3 /
- # RA05 : additional resistor for D00 to D02 input. <Not assembled> / see 1-4 /
- # RA04 : additional resistor for D03 to D05 input. <Not assembled> / see 1-4 /
- # RA03 : additional resistor for D06 to D07 input. <Not assembled> / see 1-4 /
- # RA02 : additional resistor for D10 to D12 input. <Not assembled> / see 1-4 /
- # RA01 : additional resistor for D13 to D15 input. <Not assembled> / see 1-4 /
- # RA00 : additional resistor for D16 to D17 input. <Not assembled> / see 1-4 /
- # U4 : Output device in the socket. <74LS04> / see 1-4 <Note-3>/
- # RA28 : pull-up resistor for Q0 to Q3 output. <Not assembled> / see 1-4 /
- # R3 : pull-up resistor for STB output. <Not assembled> / see 1-4 /

1-6. Settings on the board

1-6-1. BASE ADDRESS

DIO-216PC104 appears as a 16-byte block of registers within the host CPU's I/O address space. This address block must not conflict with other system I/O devices.

You can program the on-board switches SW1, SW2, and SW3 as BASE ADDRESS of the board.

These hex-a-decimal defined switches are set to SW1=0, SW2=1, SW3=C at the factory of MICRO SCIENCE, that define the BASE ADDRESS to "01C0" hex.

DIO-216PC104 occupies upper 16 byte address from the BASE.

See section 2-2 for more information.

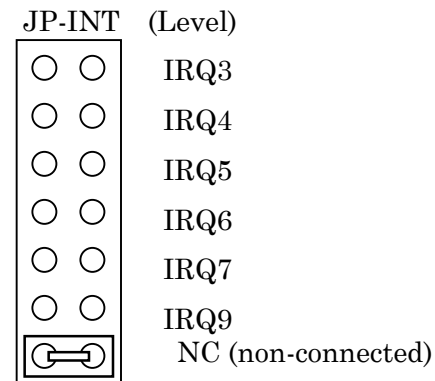
Figure 1-6A. Setting the BASE ADDRESS

Address Line →	AB15 to AB12	AB11 to AB08	AB07 to AB04	AB03 to AB00
On-board Hex-a-decimal → Switches	SW1	SW2	SW3	on-board logic decoded for multiple ports
Factory setting →	0	1	C	(F to 0)

1-6-2. Interrupt Level

Detecting the change state of specified inputs, DIO-216PC104 can cause an interrupt request to the CPU. Select the interrupt level by the jumper-switch "JP-INT", and program Write (BASE+EH) register to enable the state. See section 2-5 for the details.

Figure 1-6B. select the Interrupt Level.



1-6-3. Output Logic Polarity

Set "Bit-1" of switch "S-POL" for "Q0 to Q3", and set "Bit-2" of switch "S-POL" for "STB" as a Logic Polarity selection. See section 1-4 <Note-1> for more information.

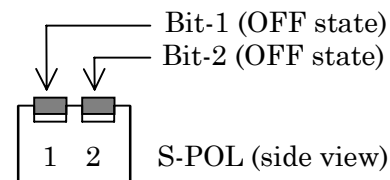


Table 1-6.

S-POL	Slect Logic Polarity		Output
	Set to "OFF"	Set to "ON"	
Bit-1	Negative	Positive	Q0 to Q3
Bit-2	Negative	Positive	STB

1-7. Digital Input Connector

16-bits Parallel Digital Inputs are available on 40-pin FRC-type male connector CN1 on the board as illustrated in Figure 1-5.

The plug is also provided for general purpose, come with the board.

Figure 1-7. Digital Input Connector CN1 pin assignment

Function	Sign	Pin assign		Sign	Function
Digital input 00	D00(A)	1	O O	2	D00(B) Digital input 00
01	D01(A)	3	O O	4	D01(B) 01
02	D02(A)	5	O O	6	D02(B) 02
03	D03(A)	7	O O	8	D03(B) 03
04	D04(A)	9	O O	10	D04(B) 04
05	D05(A)	11	O O	12	D05(B) 05
06	D06(A)	13	O O	14	D06(B) 06
07	D07(A)	15	O O	16	D07(B) 07
Digital input 10	D10(A)	17	O O	18	D10(B) Digital input 10
11	D11(A)	19	O O	20	D11(B) 11
12	D12(A)	21	O O	22	D12(B) 12
13	D13(A)	23	O O	24	D13(B) 13
14	D14(A)	25	O O	26	D14(B) 14
15	D15(A)	27	O O	28	D15(B) 15
16	D16(A)	29	O O	30	D16(B) 16
17	D17(A)	31	O O	32	D17(B) 17
		33	O O	34	
		35	O O	36	
		37	O O	38	
		39	O O	40	

<Note.1> All inputs are isolated from the PC/104 bus with the photo-coupler.

<Note.2> Blank signed pins are not connected any where.

<Note.3> On-board bracket : Model=HIF3FC-40PA-2.54DSA /made by HIROSE/
 Plug : Model=HIF3BA-40DA-2.54R(11) /made by HIROSE/

1-8. Digital Output Connector

Digital Outputs are available on a 10-pin FRC-type male connector CN2 on the board as illustrated in Figure 1-5.
All outputs have the capability for 10 TTL load.

See section 2-8 for programming.

The plug is also provided for general purpose, come with the board.

Figure 1-8. Digital Output Connector CN2 pin assignment

Function	Sign	Pin assign		Sign	Function
Digital output Q0	Q0	1	O O	2	DG
Q1	Q1	3	O O	4	DG
Q2	Q2	5	O O	6	DG
Q3	Q3	7	O O	8	DG
Strobe output	STB	9	O O	10	DG
					GND

<Note.1> DGs are the Digital Common.
They are connected each other on the board.

<Note.3> On-board bracket : Model= HIF3FC-10PA-2.54DSA /made by HIROSE/
Plug : Model= HIF3BA-10DA-2.54R(11) /made by HIROSE/

Section 2. General Programming

2-1. General Programming Information

Handling

DIO-216PC104 appears to the host PC/104 bus CPU as a block of contiguous 16 hardware registers mapped within the I/O address space.

These registers control the operation of DIO-216PC104 as long as they are accessed using 16bit I/O addressing with each 8bit data transfers.

These registers include Reset-board, General Purpose Digital I/O, watching operation command, Interrupt, and Status.

Operation

Entire information for programming are specified and explained in order as follows.

(section 2-1)

General software sequences for reading input, writing output, setting the watch condition, and Interrupt control.

(section 2-2 to 2-8)

The functions of each register. These are the elements for programming.

----- Typical software sequence -----

(1)

Read input, and Write output.

```
Outp (BASE+0x8, Dout) ; /* update Q0 to Q3 */
CD0 = inp (BASE+0x0) ; /* Read current input 00 to 07 */
CD1 = inp (BASE+0x1) ; /* Read current input 10 to 17 */
TD0 = inp (BASE+0x8) ; /* Read latched input 00 to 07 */
TD1 = inp (BASE+0x9) ; /* Read latched input 10 to 17 */
```

(2)

Interrupt by detecting the change state.

(with watching.)

```
Board-ID = inp (BASE+0xF) ; /* software reset */
Outp (BASE+0x0, W0) ; /* specify the inputs to watch */
Outp (BASE+0x1, W1) ; /* specify the inputs to watch */
Outp (BASE+0xE, 0xC0) ; /* start watching, interrupt enable */
```

(3)

Polling for detecting the change state.

(with watching.)

```
Board-ID = inp (BASE+0xF) ; /* software reset */
Outp (BASE+0x0, W0) ; /* specify the inputs to watch */
Outp (BASE+0x1, W1) ; /* specify the inputs to watch */
Outp (BASE+0xE, 0xC0) ; /* start watching, interrupt disable */
While ((inp(BASE+0xE) & 0x80) == 0x80) ; /* Detect change state */
```

2-2. I/O Register Map

DIO-216PC104 appears as a 16-byte block of registers within the host CPU's I/O address space. This address block must not conflict with other system I/O devices.

You can program the on-board switches SW1, SW2, and SW3 as BASE ADDRESS of the board.

These hex-a-decimal defined switches are set to SW1=0, SW2=1, SW3=C at the factory of MICRO SCIENCE, that specify the BASE ADDRESS to "01C0" hex.

DIO-216PC104 occupies upper 16 byte address from the BASE.

See figure 1-5 for the location of the board.

Figure 1-6A. Setting the BASE ADDRESS

Address Line →	AB15 to AB12	AB11 to AB08	AB07 to AB04	AB03 to AB00
On-board Hex-a-decimal Switches →	SW1	SW2	SW3	on-board logic decoded for multiple ports
Factory setting →	0	1	C	(F to 0)

Table 2-2. DIO-216PC104 Register Assignment. (All the port consist of 8bit.)

I/O Address	Direction	Description	Refer to
BASE +FH	Read	Reset Board, and get ID.	Section 2-3
	Write		
BASE +EH	Read	Read change state flag.	Section 2-6
	Write	Start watching, and Interrupt control.	Section 2-5
BASE +DH to BASE +AH			
BASE +9H	Read	Read latched input D10 to D17.	Section 2-7
	Write		
BASE +8H	Read	Read latched input D00 to D07	Section 2-7
	Write	General purpose Digital output (4-bits, latched)	Section 2-8
BASE +7H to BASE +2H			
BASE +1H	Read	Read current input D10 to D17	Section 2-7
	Write	Write mask data for watching input D10 to D17	Section 2-4
BASE +0H	Read	Read current input D00 to D07	Section 2-7
	Write	Write mask data for watching input D00 to D07	Section 2-4

	Not-used
--	----------

2-3. Reset the Board, and get ID

```
Board-ID = inp (BASE+0xF) ; /* Reset the Board */
```

Read (BASE+FH) Register cause the board reset.

All registers of the board must be initialized except for the last values of General Purpose Digital Output described in section 2-8.

The watching operation process shall be broken.

Where “rst” is the ID that depend on the board, “1CH” for DIO-216PC104.

Table 2-3. Read (BASE+FH) Register Bit Field.

Bit	Description
B7	1CH is the ID for DIO-216PC104.
B6	
B5	
B4	
B3	
B2	
B1	
B0	

2-4. Mask the inputs to watch

```

outp (BASE+0x0, W0) ; /* specify the (BASE+0H) input to watch */
outp (BASE+0x1, W1) ; /* specify the (BASE+1H) input to watch */

```

Write (BASE+0H) and (BASE+1H) register specifies the inputs to be watched as a mask.
See next section 2-5 for watching.

Where 2nd time, update to specify cause stop the watching, too.

Table 2-4A. Write (BASE+0H) Register Bit Field.

Bit	Term	"=1" specifies	"=0" specifies	on Reset
B7	for "D07" of (BASE+0H) input	to be watched	not to be watched	0
B6	for "D06"			0
B5	for "D05"			0
B4	for "D04"			0
B3	for "D03"			0
B2	for "D02"			0
B1	for "D01"			0
B0	for "D00"			0

Table 2-4B. Write (BASE+1H) Register Bit Field.

Bit	Term	"=1" specifies	"=0" specifies	on Reset
B7	for "D17" of (BASE+1H) input	to be watched	not to be watched	0
B6	for "D16"			0
B5	for "D15"			0
B4	for "D14"			0
B3	for "D13"			0
B2	for "D12"			0
B1	for "D11"			0
B0	for "D10"			0

2-5. Watching and Interrupt

```
outp (BASE+0xE, icc) ; /* start watching, and interrupt control */
```

Write (BASE+EH) register specifies the watching start, change state flag clear, and interrupt control.

Table 2-5. Write (BASE+EH) Register Bit Field.

Bit	Term	"=1" specifies	"=0" specifies	on Reset
B7	Interrupt control. (#1)	Enable	Disable	0
B6	Flag clear and watching start. (#2)	Do.	Not do.	0
B5	Not used.			0
B4				0
B3				0
B2				0
B1				0
B0				0

(#1) : Interrupt shall be shot when the change state is detected.

Interrupt pulse to the PC/104 bus is 500ns width, and selected by "JP-INT" on the board illustrated in figure 1-5 & 1-6B.

(#2) : Change state flag shall be cleared and new watching shall be started.

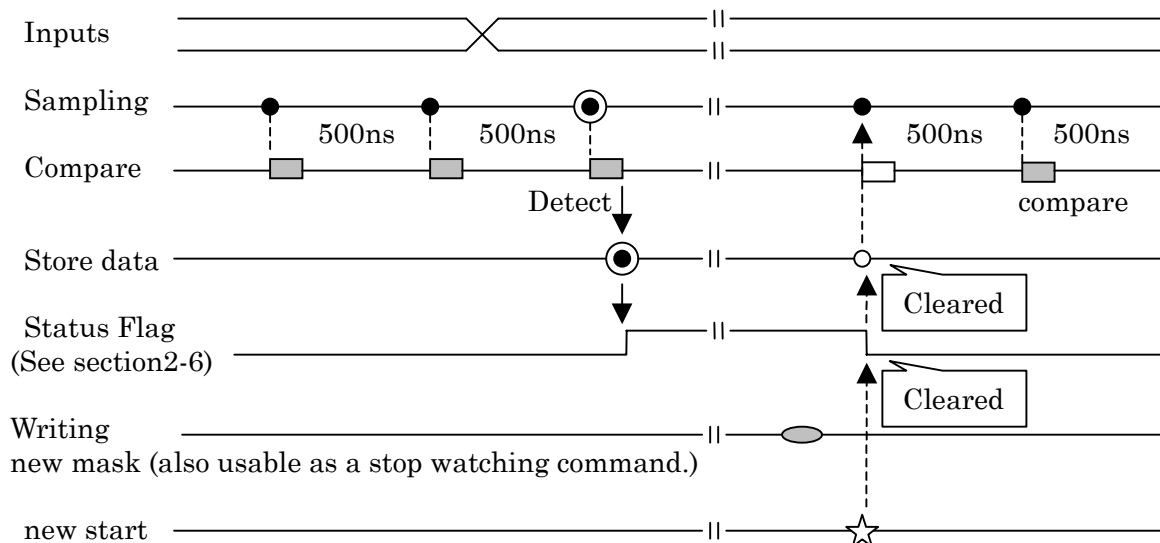
See next section 2-6 for getting the flag.

Watching operation.

Once watching is started, all inputs shall be sampled every 500ns. They shall be compared with the last reading and the mask data.

Detecting the change state with any input cause store data, set the flag, and work interrupt if it has enabled. New watching shall be started after writing mask data including stop watching.

Figure 2-5. Watching operation.



2-6. Read Status Flag

```
sts = inp (BASE+0xE) ; /* Get status Flag */
```

Change state flag shall be read from the (BASE+EH) Register.

The flag shall be cleared with the watching start as described in previous section 2-5.

Table 2-6. Read (BASE+EH) Register Bit Field.

Bit	Term	"=1" specifies	"=0" specifies	on Reset
B7	Change state flag	Detected	Not detected	0
B6	Not used.			0
B5				0
B4				0
B3				0
B2				0
B1				0
B0				0

2-7. Read inputs

CD0 = inp (BASE+0x0) ; /* Read current input D00 to D07 */
 CD1 = inp (BASE+0x1) ; /* Read current input D10 to D17 */

Current inputs shall be read from the
 (BASE+0H) and (BASE+1H) Register.

Table 2-7A. Current input register bit field.

Bit	Read (BASE+0H) Register	Read (BASE+1H) Register
B7	Current input “D07”	Current input “D17”
B6	“D06”	“D16”
B5	“D05”	“D15”
B4	“D04”	“D14”
B3	“D03”	“D13”
B2	“D02”	“D12”
B1	“D01”	“D11”
B0	“D00”	“D10”

Read Latched Input

LD0 = inp (BASE+0x8) ; /* Read latched input d00 to d07 */
 LD1 = inp (BASE+0x9) ; /* Read latched input d10 to d17 */

Latched inputs shall be read from the
 (BASE+8H) and (BASE+9H) Register.
 They shall be latched only once at detecting
 the 1st change state of specified inputs, next
 changes are ignored.

They are cleared by the new watching start,
 software reset, and power-on hardware reset
 timing. See figure 2-5 for details.

Table 2-7B. Latched input register bit field.

Bit	Read (BASE+8H) Register	Read (BASE+9H) Register	on Reset
B7	Latched input “d07”	Latched input “d17”	0
B6	“d06”	“d16”	0
B5	“d05”	“d15”	0
B4	“d04”	“d14”	0
B3	“d03”	“d13”	0
B2	“d02”	“d12”	0
B1	“d01”	“d11”	0
B0	“d00”	“d10”	0

2-8. Update Outputs

```
outp (BASE+0x8, Qout) ; /* Output Q0 to Q3 */
```

Write (BASE+8H) register updates the output Q0 to Q3.

They are TTL level (74LS04) , and latched. See figure 1-4c(in section 1-4) for the circuit.

Table 2-8. Write (BASE+8H) Register Bit Field. / with setting to **Negative Logic** . /

Bit	Term	"=1" specifies	"=0" specifies	on Reset
B7	Not used.	TTL " Low "	TTL " High "	<Note-1> <Note-2>
B6				
B5				
B4				
B3	Output "Q3"			
B2	"Q2"			
B1	"Q1"			
B0	"Q0"			

<Note-1>

Logical Polarity is set to Negative with setting the switch S-POL to "OFF" on shipping cause all outputs to TTL high state at the hardware reset in the power-on process. See section 1-6-3 for settings. Typical 100ms width high state shall be appear on all outputs at the hardware reset in the power-on process before set to Low state on Positive Logic with setting the switch S-POL to "ON".

This is a character of the circuit.

<Note-2>

Latched output Q0 to Q3 are not cleared by the software reset command, but cleared by the hardware reset in the power-on process.

<Note-3>

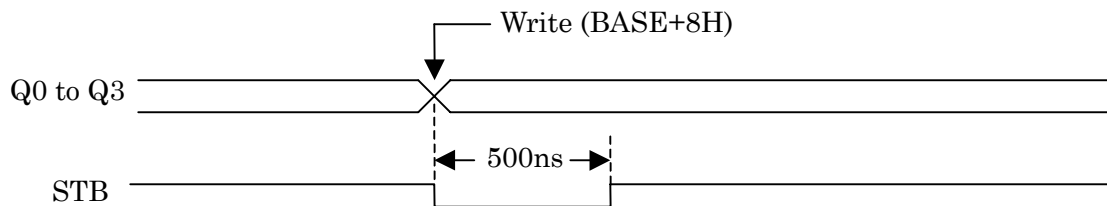
Open collector level is also available with replace the 74LS04 to 74LS06 in the socket. Strobe output "STB" belongs to that.

Strobe Output

Typical 500ns width strobe pulse shall be appear on the "STB" output at the writing (BASE+8H) register as an output update.

The Logical Polarity of strobe output is also specifies by the switch "S-POL", see section 1-6-3 for the settings.

Figure 2-8. "Q0 to Q3" and "STB" output timing.



Section 3. Maintenance and Appendix

3-1. Trouble Shootings

Reconfirm.

The DIO-216PC104 supplied by MICRO SCIENCE is fully inspected and tested. If it doesn't work on your system, reconfirm following issues.

- (1) Check the I/O BASE address specified by the on-board switch SW1, SW2, and SW3. On the IBM PC/AT compatible system, the I/O address must be mapped between "0H" to "3FFH" or the image of this range except for the occupied address by the other devices or the peripherals.
- (2) Debug your software or applications. For example, if the Interrupt level is correct or if occupied by any other devices.
- (3) Be careful to connect the input, and DIO-216PC104 requires appropriate power supply to force the input "ON" current. See section 1-4 for details.

What's wrong?

Fill in and send (Letter, Fax, or Email) the Q&A form to MICRO SCIENCE where you didn't find anything wrong.

Although we will study about your system and answer by the letter what you should do, we don't write or debug application software.

Sorry, we won't answer with any language but Japanese on the phone. Please write us Japanese or English.

Replace the Board or Repair for free.

MICRO SCIENCE will replace or repair the Board for free which are after examination disclosed to the satisfaction of MICRO SCIENCE to be thus defective, for a period within one year of shipment. This warranty shall not apply which have been subject to misuse, negligence, or accident. See "Caution/Warranty" for details in page-3.

Repair the Board.

MICRO SCIENCE will repair, calibrate, or test the Board on request. These products should have to prepaid the transportation at MICRO SCIENCE. Be sure, give us the information with the products, maybe Q&A form is useful for the report.

Then user have to pay the proper cost in few weeks according to the bill after accept the returned products.

Q & A form (in English or Japanese)

To:
MICRO SCIENCE., Co. LTD
Customer Support Div
2-37-12, Nishiogi-kita,
Suginami-ku,
Tokyo, Japan

From:

Fax: +81-3-3301-5593
Email: gas@microscience.co.jp

Fax:
Email:

DIO-216PC104	serial # =	Purchase Date:
Preferences on- Board	SW1 =	JP-INT = 3, 4, 5, 6, 7, 9
	SW2 =	S-POL (Bit-1) = OFF, ON
	SW3 =	S-POL (Bit-2) = OFF, ON
Other Devices In the system	Product:	
	Occupied Resources: (I/O Address =), (Interrupt =)	
System Information	CPU:	
	OS :	
Software	Language:	
	Compiler:	

(Information)

<Note> MICR SCIENCE does not answer on phone with any language but Japanese.